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Tunnel FinFET CMOS Inverter with Very Low Short-Circuit Current for Ultra-Low Power IoT Application

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Abstract

We have demonstrated operation of a CMOS inverter consisting of Si tunnel FinFETs. Both p- and n-type tunnel FinFETs are successfully fabricated and operated on the same silicon on insulator (SOI) wafer. Very low short-circuit current and clear voltage input-output characteristics are obtained.

1. Introduction

Because the tunnel field-effect transistor (TFET) utilizes band-to-band tunneling (BTBT) of semiconductors as an operation principle, a steeper subthreshold swing (SS) than that in conventional metal oxide semiconductor (MOS) FETs is possible [1,2]. Under operation of reverse-bias condition of a p-i-n junction of the TFET channel, off-current of the TFET can be maintained at very low (lower than a few pA/μm) value [3]. This is great advantage for ultra-low power (ULP) Internet of Things (IoT) applications.

In this study, we demonstrate Si tunnel FinFET CMOS inverter operations. The scaled fin channel can effectively suppress the SS and off-current values [4-6]. Lower short-circuit current than that for MOSFET CMOS inverter and clear input-output voltage operation are obtained. By using simplified capacitance measurement and simulation, we show advantage of epitaxical channel TFET on the TFET inverter operation.

2. Experimental setup

Figure 1 shows a model of Si tunnel FinFET in the present study. An epitaxially grown thin channel layer is inserted at the top of the fin-channel, which is the key technology of the tunnel FinFET for boosting on-current [4-6]. The process flow of the CMOS tunnel FinFETs is based on a source/drain-first FET process on the silicon on insulator (SOI) wafer. (**Fig. 2**) The source and drain are preferentially created by ion implantations (I/I). Source and drain wells are separately ion-implanted for one TFET. For inverter fabrication, source of n-TFET and drain of p-TFET are initially created, followed by I/I of drain of n-TFET and source of p-TFET. **Fig. 3** shows cross-sectional TEM image of fin channel. An undoped thin Si channel is epitaxially grown on the wafer after dopant activation and surface cleaning. The stacked epitaxial channel interface is outcropped at the sidewall by reactive ion etching. High-k gate insulator (HfO_2, EOT = 1.3 nm) and gate electrode (TiN, 30 nm) are deposited covering three-dimensional channel [5].

3. Results and discussion

Fig. 4 shows comparison of typical transfer characteristics of fabricated TFETs for (a) conventional, (b) parallel-plate (PP) type, and (c) epitaxial channel fin-type TFETs. By improving the TFET architecture, ON-current and SS values can be improved step-by-step. However current value for n-type tunnel FinFET is smaller than that of p-type one. For fabrication of CMOS inverter, multiple-number fin channel is adopted to compensate the current mismatch between the n- and p-type TFETs. (**Fig. 5**) As for the single fin channel, gate length (L_G) is 0.1-10 um, fin width is 100 nm, and source-gate overlapped length is 1/2 of L_G. **Fig. 6** shows V_{IN}-V_{OUT} characteristics of CMOS inverters consisting of tunnel FinFETs. Clear switching feature is realized. **Fig. 7** shows comparison of short-circuit currents (I_{SC}) in tunnel FinFET and MOSFET CMOS inverters. Peak and stand-by value of I_{SC} for TFET CMOS inverter is drastically reduced compared to that for MOSFET. The I_{SC} reduction is effective to reduce power consumption of the TFET CMOS inverter, which is one big advantage of TFET circuit. As for the I_{SC} increase at low V_{IN} region for tunnel FinFET inverter, this phenomenon originates from the ambipolar current of n-type TFET. Therefore, this excess I_{SC} can be reduced by design optimization of drain side of n-TFET. **Fig. 8** shows a CMOS inverter simulation for conventional TFETs by using a TFET compact model [7]. V_{OUT} notch and long discharge tail appear in V_{OUT} transient. This undesirable features are caused by significant impact of the total gate capacitance (C_{GG}) to S/D under small current drivability of TFETs [7,8]. Total gate capacitance of the conventional-type TFET is dominated by drain side capacitance. In the case of CMOS inverter, drain of both p- and n-TFETs are connected to V_{OUT} terminal, and low drive current to charge/discharge large drain capacitances is a problem for TFET inverter. **Fig. 9** shows measured and simulated C–V characteristics of the p-TFET featuring ultrathin epitaxial channel. By inserting the undoped epitaxial channel and gate-source overlapped area, which acts as parallel-plate tunnel capacitor, source side capacitance increases with increasing overlapped area. Accordingly, drain side capacitance decreases with decreasing source-to-drain length (**Fig. 10**). The impact of epitaxial channel insertion effectively increases the drain current, and reduces capacitance problem, which could help high performance TFET inverter operation.

4. Summary

CMOS inverter consisting of Si tunnel FinFETs has been experimentally demonstrated on the conventional Si platform. Very low short-circuit current and clear switching are obtained. Impact of thin epitaxial channel on the tunnel FinFET effectively increases drain current and accordingly reduces drain capacitance, which could help high performance inverter operation. These results suggest that Si tunnel FinFET CMOS inverter is suitable for ultra-low power and low cost IoT application.

Acknowledgment

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References

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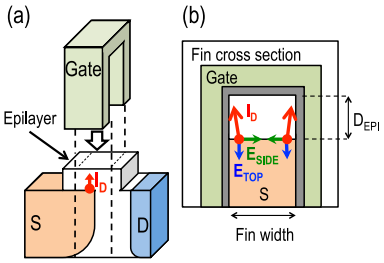

Fig. 1 Schematics of tunnel FinFET featuring ultrathin epitaxial cannel inserted between gate and source, in the present study. Inset shows channel cross-section of tunnel FinFET, indicating synthetic electric field at the source/epichannel interface.

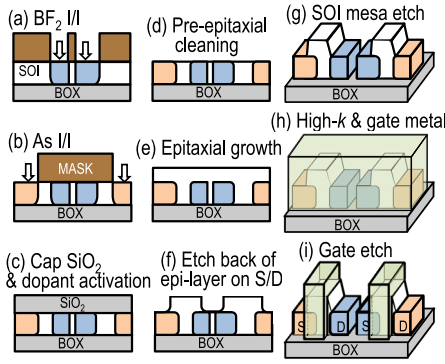

Fig. 2 Process flow of CMOS tunnel FinFETs.

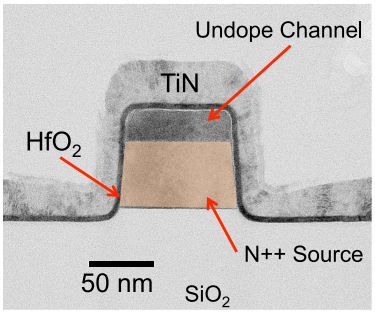

Fig. 3 Typical XTEM image of tunnel FinFET (p-type) channel.

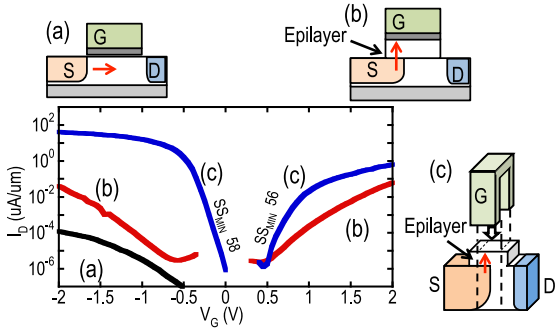

Fig. 4 Typical transfer characteristics of three TFET architectures: (a) conventional lateral type (V_D = |1| V, L_G = 1 μm), (b) parallel-plate type (V_G = |1| V, L_G = 500 nm), and (c) FinFET-like TFETs (V_D = |0.2| V, L_G = 100 nm). For conventional TFET, only p-type I_D–V_G is plotted.

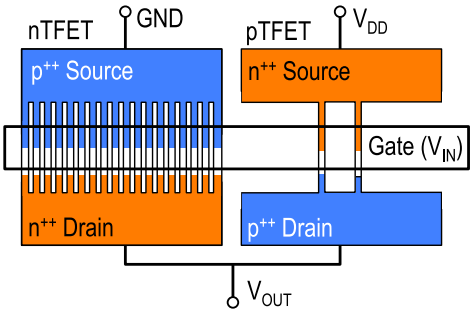

Fig. 5 Device configuration in tunnel FInFET CMOS inverter. V_{IN} is added for gate electrode. Numbers of fin channels are 2 and 18 for p- and n-type tunnel FinFETs, respectively.

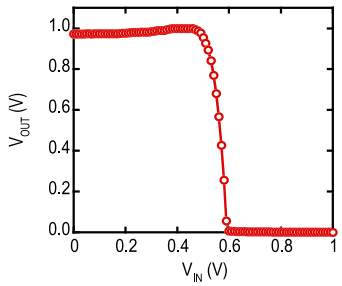

Fig. 6 Typical V_{IN}–V_{OUT} characteristics of tunnel FinFET CMOS inverter. L_G = 1 um. V_{DD} = 1 V.

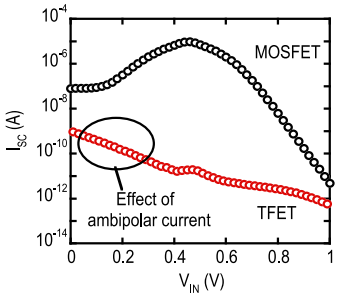

Fig. 7 Comparison of short-circuit current of MOSFET and tunnel FInFET CMOS inverters. L_G of TFETs and MOSFETs are 1 and 8 μm, respectively. V_{DD} = 1 V for both inverters.

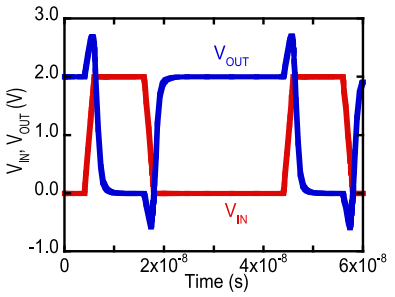

Fig. 8 Simulation of Si CMOS TFET inverter. V_{IN} = 2 V. Conventional type Si TFET is simulated [7].

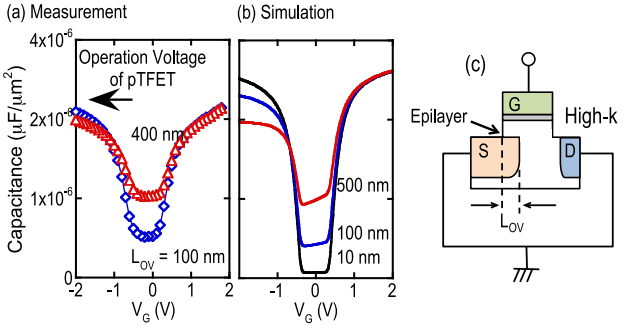

Fig. 9 Typical C–V characteristics of pTFET featuring ultrathin epitaxial channel. Variations in source-gate overlapped length (L_{OV}) exist. (a) Experimental and (b) simulation results. (c) Measurement setup.

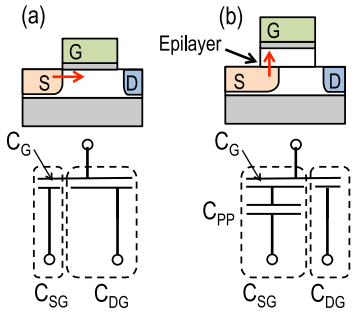

Fig. 10 Schematic capacitance distribution models for (a) conventional and (b) epitaxial channel TFETs. Distribution of source and drain capacitances are also indicated. In the case of (b), parallel-plate capacitor is inserted.