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On the Variability of Tunnel Field-Effect Transistors: Suppression of BTBT Fluctuation by Tunneling Probability Enhancement

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Abstract

We show variability suppression in TFETs thanks to tunnel probability enhancement. The tunnel probability enhancement, which is accomplished by the introduction of an isoelectronic trap (IET) into Si, improves not only I_{on} and SS but also the variability to as low as 65 % for I_{on} and 60 % for V_{th}. It is revealed that the tunnel probability enhancement contributes to the reduction of tunnel rate variation on the basis of Kane's band-to-band tunneling rate equation. The suppression is a universal tendency for TFETs; therefore, it is predicted that high tunneling rate channel technology, with Ge or III-V, as well as the IET technology, also benefits from the variability improvement.

1. Introduction

Tunnel FETs (TFETs), which can be operated with a sub-60 mV/decade subthreshold slope (SS), are one of the candidate devices for realizing low operation voltage CMOS circuits. The high resistivity of the tunnel barrier hampers the boosting of ON current in TFETs. A solution to this problem is to realize high tunneling rate; therefore, recently, high rate channel technology with Ge or III-V has been investigated [1]. As the alternative technology based on Si, the isoelectronic trap (IET) technology to enhance tunnel probability has been proposed by our group [2].

Variability is the other crucial issue for low voltage operation if the TFETs [3]. In this report, we discuss the general relationship between the variability and the tunneling probability. As a direct investigation of the relationship between the variability and the tunneling probability under the identical fabrication process and device structure, we demonstrate the variability suppression in SOI-TFETs accompanied by tunneling probability enhancement thanks to the IET. The variability suppression can be understood on the basis of the Kane's band-to-band tunneling (BTBT) rate equation.

2. Experiment and Simulation

Fig. 1(a) and (b) shows the device fabrication process and a TEM picture, respectively. We utilized a HfO_2/TaN gate with a SiO_2 interface having an EOT of 1.5 nm. The fabrication process was the same in the previous reports [2]. Fig. 1(c) shows a model of the tunneling probability enhancement by IET proposed in Ref. 2. The simulation was performed in HyENEXSS™ [4] with a non-local tunneling model [5].

3. Results and Discussion

Fig. 2 shows the variation of I_d-V_g curves of the IET- and control TFETs. Fig. 3 shows normal quantile plots for I_{on}, SS, and V_{th} variations of IET- and control TFETs with the varied L_g. The I_{on} enhancement and SS improvement originate from the tunneling probability enhancement by the IET as reported previously [2]. Fig. 4 is a summary of the variability for the cases with and without the IET. The tunnel probability enhancement by introducing the IET benefits the suppression of variability as low as 65 % for I_{on} and 60 % for V_{th}. Clearly, the variability suppression by means of the tunneling probability enhancement by the IET was demonstrated. Also, here we mention negligible change of the variability upon the L_g variation with identical channel width (Fig. 3). This is discrepant from the conventional MOSFET whose variation depends on the area of the channel by the conventional Pelgrom plot [6]. This is because pn junction at the source-side edge of the gate dominantly determines TFET performance.

To discuss the origin of the variability suppression, we performed TCAD simulation. Fig. 5 shows the mappings of the carrier generation by BTBT at the source-side edge of the gate. In this figure, we show the case of varied EOT, that is one of the possible origins of the variability, as a representative. The variation of the electric field at the BTBT position due to the EOT variation is identical for the high probability and control TFETs. On the other hand, the smaller BTBT rate variation ($\Delta G/G$) is recognized in the high probability TFETs. This fact is also valid for the other variation origins, the source I/I dose and S/G overlap. Therefore, it is supposed that the tunnel probability enhancement directly suppresses the $\Delta G/G$.

The $\Delta G/G$ variation caused by the junction electric field variation can be understood on the basis of Kane's BTBT rate equation [7]. The $\Delta G/G$ is written as in Fig. 6, in which we introduce the sensitivity coefficient S. It is clear that S decreases with decreasing tunneling rate parameter B (corresponding to increasing tunneling probability). Therefore, the higher tunnel rate is, the smaller S coefficient is. This results in variability suppression as experimentally demonstrated in this work. This is a universal relationship in TFETs; therefore, technologies realizing high tunnel rate, not only the IET technology but also Ge or III-V channel technologies, benefits variability improvement.

4. Conclusion

Suppression of the variability of TFET performance by

tunnel probability enhancement has been experimentally demonstrated with IET-TFETs as a showcase, and the suppressed variation of 65 % for I_{on} and 60 % for V_{th} are achieved. The suppression is universal for any technologies of tunnel probability enhancement including the high rate channel technology. Therefore, the probability enhancement technologies pave the way to realizing not only high current drivability but also suppressed device variability in TFETs.

Acknowledgements

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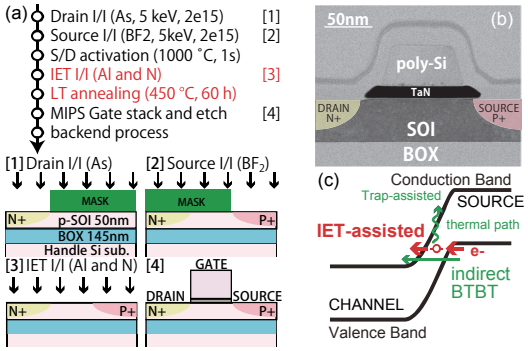

Fig. 1. (a) Process flow of the IET-TFET. The Al-N impurity complex provides the IET. The I/I was performed with the energy of 15 keV and the dose of 5×10^{12} /cm^2 (for both Al and N). (b) A typical TEM picture of TFETs. (c) A schematic band diagram of a model of IET-assisted tunneling [2].

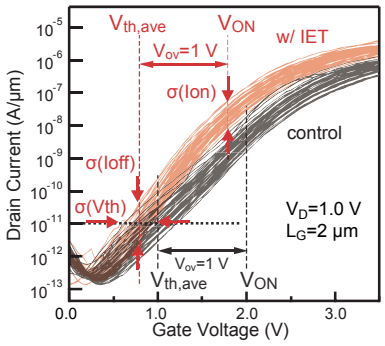

Fig. 2. Variation of I_d-V_g curve. First, $V_{th,ave}$ is defined as V_G at $I_{off,ave}=1\times10^{-11}$ A/μm. Then, V_{ON} is defined as $V_{th,ave}$ + 1 V and is used for I_{on} definition subsequently. SS is defined as the average SS in the I_d range from 1×10^{-11} to 1×10^{-10} A/μm.

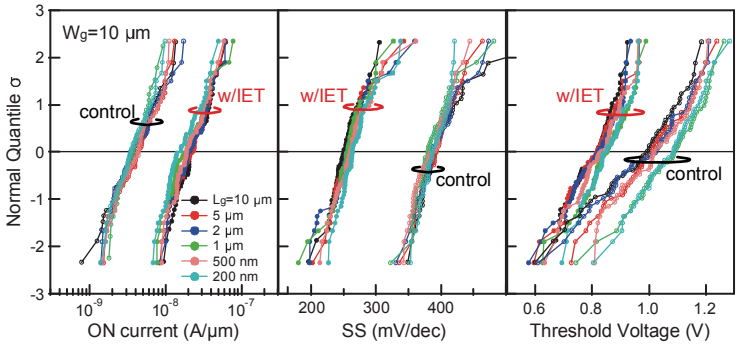

Fig. 3. Normal quantile plots of I_{on}, SS, and V_{th} of the IET- and control TFETs. IET enhances I_{on} and improves SS, as previously reported [2]. No L_g-dependence of the variability was observed. The I_{on} and V_{th} variations were suppressed thanks to tunnel probability enhancement by the IET.

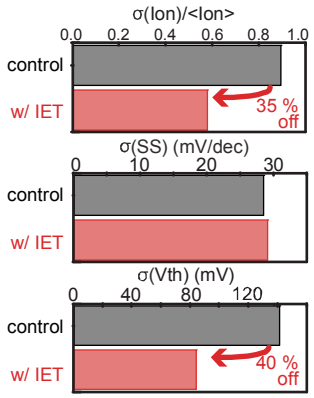

Fig. 4. A summary of the variability suppression. This is of the L_g=2μm devices, as a representative.

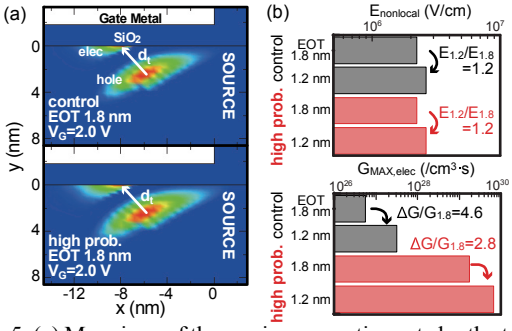

Fig. 5. (a) Mappings of the carrier generation rate by the tunneling with EOT variation as a possible origins of the variability, simulated by TCAD. (b) The change of the electric field strength and the carrier generation rate.

$$G = AE^{\gamma}\exp\left(-\frac{B}{E}\right)$$
$$\Delta G = \frac{\partial G}{\partial E}\Delta E$$
$$\frac{\Delta G}{G} = \left(\gamma + \frac{B}{E}\right)\frac{\Delta E}{E} \equiv S\frac{\Delta E}{E}$$

G : tunneling rate
A, B : probability params
γ : 2 for direct, 2.5 for indirect
E : electric field strength
S : sensitivity coefficient

Fig. 6. The relation between the electric field variation and the tunneling rate variation derived from the Kane's tunneling rate equation. The higher tunnel rate provides the smaller variation. This is a universal relationship in TFETs.