Extended Abstracts of the 2016 International Conference on Solid State Devices and Materials, Tsukuba, 2016, pp53-54

A-7-02

Drain-Bias Dependency on Statistical Variability for Tunnel Field-Effect Transistors

Woo Young Choi, Song Hun Choi, Jang Woo Lee, and In Huh

Department of Electronic Engineering, Sogang University
35 Baekbeom-ro (Sinsu-dong), Mapo-gu, Seoul 04107, Republic of Korea

Abstract

The drain bias effects on statistical variability characteristics for double-gate (DG) tunnel field-effect transistors (TFETs) are discussed in comparison with MOSFETs. The unique variability depending on drain bias is analyzed by using full three-dimensional simulation which is performed with dominant statistical variation sources such as line-edge roughness (LER), random dopant-fluctuation (RDF) and work-function variation (WFV).

1. Introduction

A tunneling field-effect transistors (TFET) has attracted much attention thanks to less than *SS* of 60 *mV*/decade at room temperature as well as good CMOS process compatibility [1]. However, CMOS fabrication processing indispensably compelled to induce the imperfect matching-characteristics along the devices, so-called statistical variability (*SV*). And it has become one of the major concerns to device scaling and integration beyond the 45-*nm* technology node, since *SV* reaches more than 50% of the total variability from this process [2, 3]. From this point of view, the impact of drain bias for TFETs in terms of *SV* is essential for commercialization of *LSTP* IC-applications. To the best of our knowledge, only few studies for drain bias dependency of TFETs such as *DIBT* (drain induced barrier thinning) which is another important figure of merit for device performance has been reported and even its *SV* characteristics has not been proceed yet [4]. In this letter, the impact of the drain-bias on *nano*-scaled TFET (i.e. 24 *nm*) V_{th}, *DIBT* and sub-threshold swing (*SS*) variability is precisely studied by commercial full-3*D* simulation, taking into account all relevant principal *SV* sources: line-edge roughness (LER), random dopant fluctuation (RDF) and work-function variation (WFV) [5].

2. Simulation results and discussion

In our simulation, only n-channel double-gate (DG) MOSFETs and TFETs were considered for simplicity as shown in Fig 1. Detailed physical parameters are described in Table 1. A total of 200 device structures of DG TFETs and MOSFETs have been generated, respectively. Fig. 2 shows the simulated transfer curves of DG TFETs and MOSFETs under the influence of total variation (LER+RDF+WFV) and their simulation results are presented in Fig. 3, 4 and 5. Fig. 3 and 4 summarizes the simulation results using criteria of V_{th} for I_D = 1 nA/μm. Also, Fig. 5 summarizes the simulation results for DIBT using various V_{th} criteria to check the trends in entire I_D regime.

As a result, two noticeable results are confirmed by 3D simulation. First, TFETs and MOSFETs show completely opposite drain dependency for σV_{th} and σSS as shown in Fig. 3. For all variation sources and total variation, TFETs have mitigated σV_{th} and σSS as V_{DS} increases, however, MOSFETs show worsened their electrical parameters (i.e. σV_{th} and σSS). Also TFETs show relatively larger discrepancy between V_{DS} = 0.1 V and V_{DS} = 1 V especially for σSS. Second, as shown in Fig. 5a and b, as I_D increases, TFETs show sharp increasing for DIBT and σDIBT unlike MOSFETs which show relatively constant DIBL and σDIBL.

These results come from the drain bias dependency of inversion layer formation. Unlike MOSFETs which the inversion layer is connected to source side, the case of TFETs is connected to drain side because inversion charges are originated from the drain by thermionic emission mechanism. Thus, drain bias has stronger influence for TFETs than MOSFETs. For further analysis, gate-to-source capacitances (C_{GS}) and gate-to-drain capacitances (C_{GD}) as a function of V_{DS} and V_{GS} are extracted as shown in Fig. 6a, b and c. V_{inv} is defined as V_{GS} when the inversion layer is formed and extracted based on the previous work and the influence of V_{DS} for V_{inv} can be confirmed in Fig. 6a. As V_{DS} decreases, V_{inv} also decreases because the thermionic emission barrier between channel and drain decreases. Similarly as V_{DS} increases, V_{inv} increases because inversion charges are pulled back to drain. And the influence of inversion layer for TFETs can be confirmed in Figs. 6b and c. As the inversion layer is formed earlier, due to the reduced channel resistance, lateral electric field induced from drain penetrates into the source/channel junction where tunneling occurs easily. And as V_{DS} increases, channel charges decrease, thus increased channel resistance screens lateral electric field penetration into the source/channel junction. This phenomenon can be confirmed in Fig. 6b that C_{GS} saturates as V_{DS} increases. And the inversion layer formation causes channel potential pinning and weakens the controllability of gate for source/channel junction. This fact also can be confirmed in Fig. 6c that C_{GS} decreases significantly after V_{inv}. As a result, we can conclude that increase in channel charges (i.e.: inversion layer formation) makes TFETs more vulnerable to *SV* by two reasons: increased sensitivity for lateral field by V_{DS} and weakened gate controllability for source/channel junction.

3. Summary

The drain bias dependency on variability characteristics for TFETs has been studied for the first time. TFETs show different, strong and complex drain bias dependency on variability characteristics than MOSFETs. As a result, for circuit application of TFETs, more careful and different treatments for drain bias than MOSFETs are needed. Our findings could provide useful insight for variation-tolerant design of TFETs.

Acknowledgements

This work was supported in part by the NRF of Korea funded by the MSIP under Grant NRF-2015R1A2A2A01003565 (Mid-Career Researcher Program), NRF-2015M3A7B7046617 (Fundamental Technology Program) and in part by the MOTIE/KSRC under Grant 10044842 (Future Semiconductor Device Technology Development Program).

References

[1] W. Y. Choi *et al.*, *IEEE Electron Device Lett.*, vol. 28, no. 8, pp. 743–745, Aug. 2007. [2] A. R. Brown *et al.*, *IEEE Trans. Electron Devices*, Vol.54, No.11, pp.3056-3063, 2007. [3] H. Aikawa *et al.*, *Symposium on VLSI Technology*, pp. 90-91, 2008. [4] L. Liu et al., *IEEE Trans. Electron Devices*, vol. 59, no. 4, pp. 902–908, Apr. 2012. [5] Sentaurus Device User Guide Version: H-2013.03, Synopsys, 2013.

TABLE I. REFERENCE DEVICE PARAMETERS

	TFETS	MOSFETS
Gate length (L_g)	24 nm	
Fin width (W_{fin})	8 nm	
Fin height (H_{fin})	12 nm	
Source doping concentration	10^{20} cm^{-3} (p-type)	10^{20} cm^{-3} (n-type)
Drain doping concentration	10^{20} cm^{-3} (n-type)	
Channel doping concentration	Intrinsic	10^{16} cm^{-3} (p-type)
Side-gate oxide thickness ($t_{ox,side}$)	0.7 nm	
Source/drain doping abruptness	1 nm/dec.	
Supply voltage (V_{DD})	1.0 V	

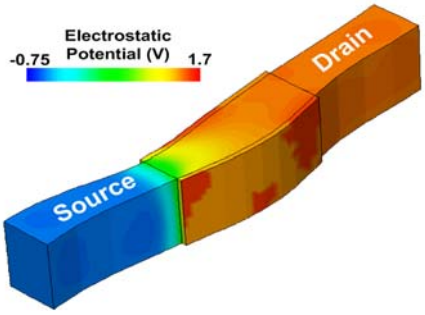

Fig. 1. One example of DG TFET showing electrostatic potential affected by statistical variation sources including LER, RDF and WFV.

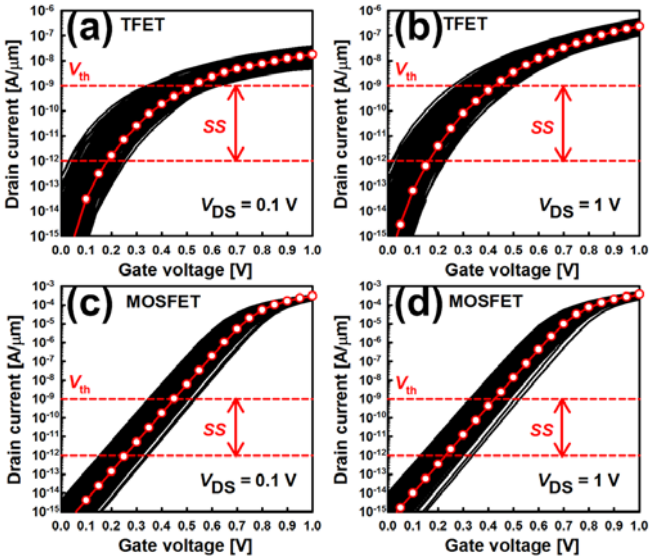

Fig. 2. Transfer curves of 200 generated DG TFETs and MOSFETs: DG TFETs under total variation in (a) V_{DS} = 0.1 V and (b) V_{DS} = 1.0 V, DG MOSFETs under (c) total variation in V_{DS} = 0.1 V and (d) V_{DS} = 1.0 V. Symbolic lines corresponding to the transfer curves of nominal devices.

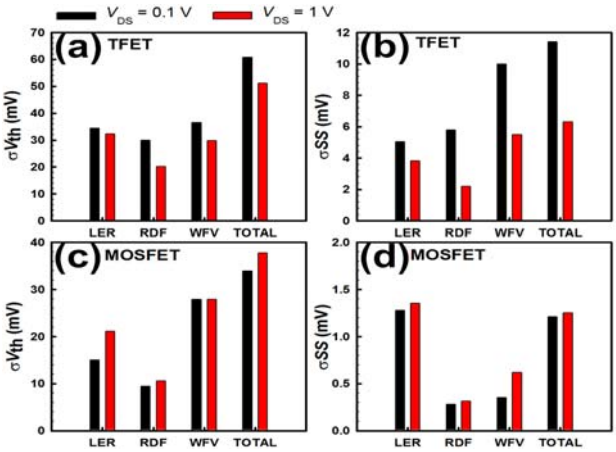

Fig. 3. LER, RDF, WFV and total variation induced (a) σV_{th}, (b) σSS for TFETs and (c) σV_{th}, (d) σSS for MOSFETs.

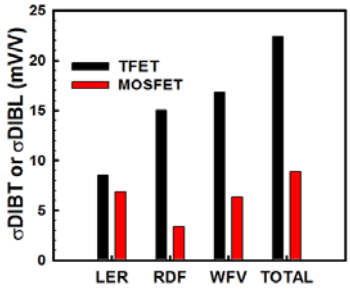

Fig. 4. LER, RDF, WFV and total variation induced σDIBT and σDIBL using criteria of V_{th} for I_D = 1.0 nA/μm..

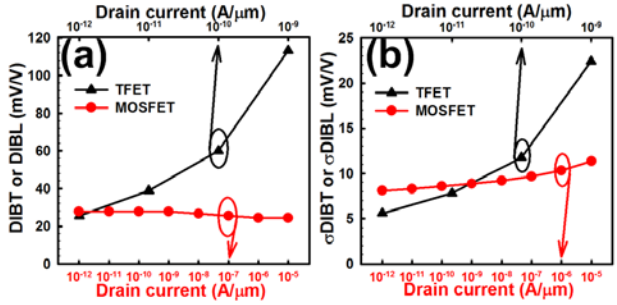

Fig. 5. Variation trends according to I_D increasing for (a) DIBT and DIBL, (b) σDIBT and σDIBL.

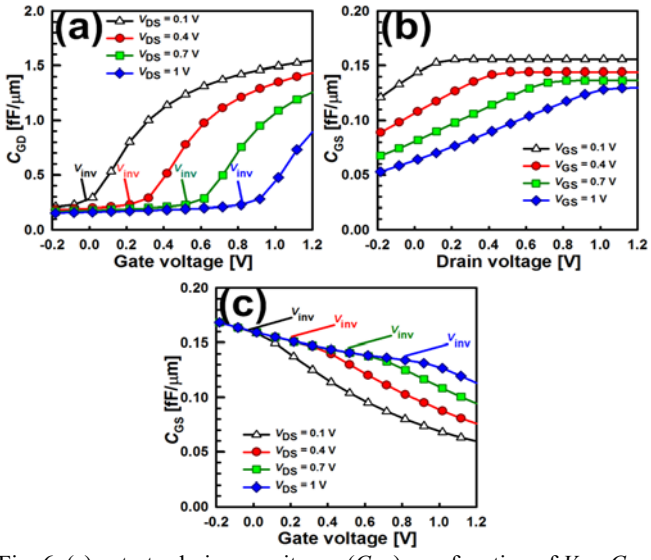

Fig. 6. (a) gate-to-drain capacitance (C_{GD}) as a function of V_{GS}, C_{GD} as a function of (b) V_{DS}, and (c) V_{GS}.