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A Study on the Correlation between SRAM Power-up State and Transistor Variation

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Abstract

The correlation between SRAM power-up state (i.e. the state 0 or 1 just after the power is turned on) and the cell transistor variation is systematically studied. It is revealed that, while both the mismatch of pFETs (pull-up) and nFETs (pull-down and access) contribute, their relative importance changes depending on the voltage ramp rate and node capacitance, due to the effects of displacement current. As a result, static retention noise margin is not well correlated with the power-up state except for limited operation conditions.

1. Introduction

Recently, physical unclonable functions (PUFs) are attracting attention. A PUF generates a random number that is specific to the device where it is embedded, by utilizing production variability. The number can be used as a "fingerprint" for identification or for encryption purposes. A typical example is SRAM PUF [1], which generates the number from the stored data in an SRAM, just after the power supply voltage is turned on. Power-up state is also important for some special non-volatile memories [2].

Power-up SRAM data depends on various factors, such as transistor mismatch, voltage ramp rate, temperature, and noise. To achieve reliable PUF design, it is important that the details of the power-up state determination process is fully understood. However, only a limited number of reports are available that directly correlate the power-up state with transistor level behavior of the SRAMs [3,4].

In this work, the power up behavior of 6T-SRAM cells was analyzed in detail. Using Monte Carlo simulation and linear classification, the contribution ratio of the three mismatch factors (pull-up, pull-down and access FETs) to determining the power-up state are quantitatively derived. The root cause for its dependence on the voltage ramp rate and node capacitance is discussed. Experimental results will be also shown.

2. Simulation and Analyses

Monte Carlo power-up transient simulations assuming only random V_{TH} variation as the source of randomness were performed for 0.18μm technology SRAM cells (Fig.1). V_{CC} was linearly ramped from zero to 0.5V, keeping V_{BL1}= V_{BL2}=V_{WL}=0, and the power-up state 0 or 1 was determined. After repeating 10000 runs, a partitioning plane in the 3-dimensional space, spanned by the mismatch values x = $V_{TH,PU1}$-$V_{TH,PU2}$, y = $V_{TH,PD1}$-$V_{TH,PD2}$ and z = $V_{TH,AC1}$-$V_{TH,AC2}$, is obtained, which best classifies the power-up states (Fig.2). The normal vector direction of the plane directly indicates the ratio of the contributions of pull-up, pull-down and access transistor mismatch to the power-up state. Mismatch of retention noise margin ΔRNM (Fig.3) is also calculated.

3. Results and Discussion

Fig.4a shows histograms of $\Delta V_{TH}=c_1x+c_2y+c_3z$, i.e. the distance from the partitioning plane, for rise time T_{RISE}=1μs. The overlap of the 0- and 1-state histograms is small, indicating that the correlation between ΔV_{TH} and the power-up state is high. Since c_1~1, the start-up state in this example is almost determined by the pFET mismatch alone. Fig.4b shows similar histograms for ΔRNM, indicating that the correlation between the power-up state and RNM is poor. Fig.5 shows the vector elements (c_1, c_2, c_3) vs T_{RISE}. As the rise time increases, nFET contributions increase. Fig.6 shows the histograms of ΔV_{TH} and ΔRNM for T_{RISE} =1ms. The much better separation of ΔRNM (Fig.6b) than Fig.4b shows that, if the V_{CC} ramping is sufficiently slow, the start-up state is in good correlation with RNM.

The above results can be explained as follows. Fig.7a shows the internal node voltage waveforms during power up for four different T_{RISE} values. As the ramping speed is increased, the voltage at which the separation between the two nodes starts becomes higher. This is due to the increase of the displacement (capacitive) current. Since no capacitance mismatch is assumed, the separation starts only after the transistor static current overcomes the displacement current. If the ramping is fast, when the separation begins, high voltage is already present and the voltage across the pFETs is substantially higher than nFETs due to the larger capacitive coupling of the internal nodes to the ground (Fig.7b). This makes the drain current of pFETs much larger than nFETs (more than one order for T_{RISE}=1μs). Hence, the power-up state is dominated by the pFET mismatch. If the ramping is slow enough, displacement current becomes not important, and low voltage static transistor characteristics determine the power-up states.

To experimentally confirm the above, an addressable SRAM cell array test structure (Fig.8), specially designed to allow V_{TH} measurements of individual transistors constituting each cell [5,6], was used. Fig.9 shows measured (c_1, c_2, c_3) vs T_{RISE}. Similar tendency as Fig.5 was confirmed, though the rise time used was extremely larger than Fig.5. The difference of the rise time range is considered to be due to the additional wire capacitance (hundreds of pF) connected to the internal nodes in Fig.8. Fig.10 shows simulated vector elements (c_1, c_2, c_3) vs additional node capacitance for T_{RISE}=10μs. As the capacitance increases, larger displacement current, as well as larger coupling of the nodes to the ground, strengthen the dominance of pFETs. The extremely slow ramping necessary to see nFET contribution in Fig.9 can be explained by this effect.

4. Conclusion

The impact ratio of pull-up, pull-down and access transistor mismatch on the power-up states depends on the ramping speed. This behavior can be explained by the balance between the static and displacement currents, as well as asymmetrical capacitive coupling of the internal nodes to the ground and V_{CC}.

Acknowledgements

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References

[1] D. E. Holcomb et al., IEEE Trans. Computers, 58, p.1198, 2009. [2] T. Mizutani et al., submitted to SSDM 2016. [3] M. Cortez et al., IEEE DFT 2012. [4] S. O'uchi et al., IEDM 2015, p.648. [5] T. Hiramoto et al., IEEE Trans. Electron Devices, 58, p.2249, 2011. [6] K. Takeuchi et al., IEEE ICMTS 2016, p.130.

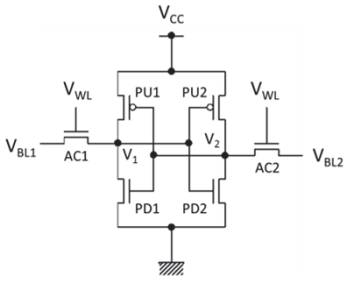

Fig.1 Transistor and voltage label definitions for a 6T SRAM.

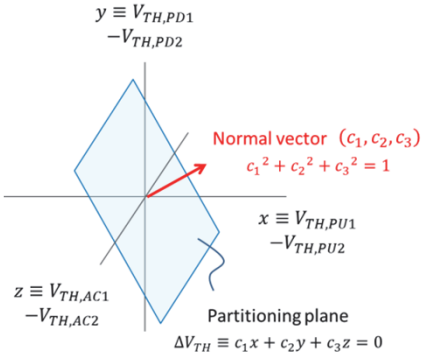

Fig.2 Concept of mismatch space partitioning.

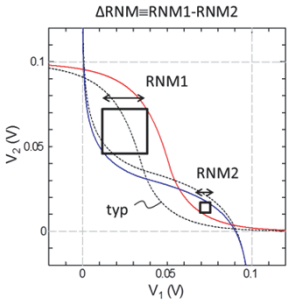

Fig.3 Retention noise margin mismatch (ΔRNM) definition. Two transfer curves are obtained at V_{BL1}=V_{BL2}=V_{WL}=0 and V_{CC}=0.1V.

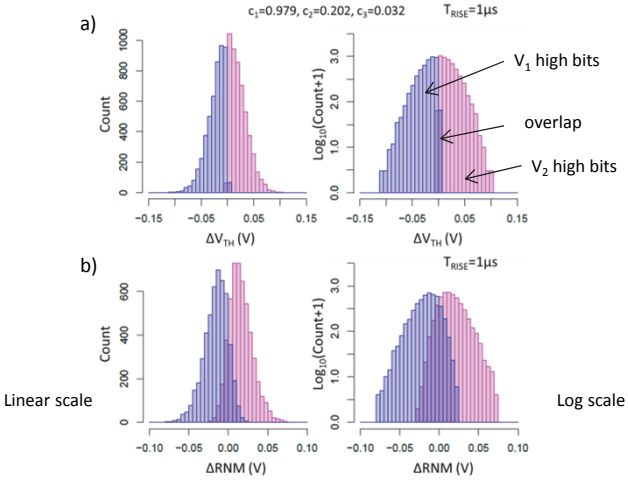

Fig.4 ΔV_{TH} and ΔRNM histograms for T_{RISE}=1μs. ΔRNM separation is poor.

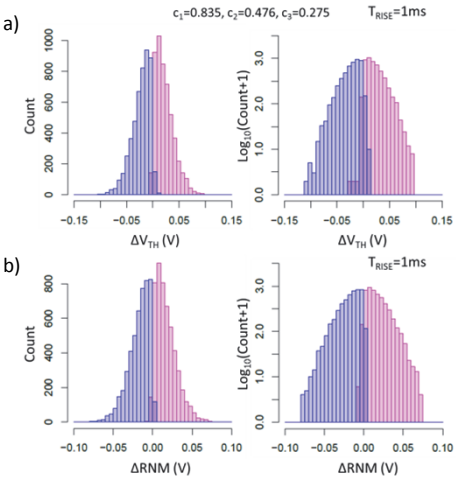

Fig.6 ΔV_{TH} and ΔRNM histograms for T_{RISE}=1ms.

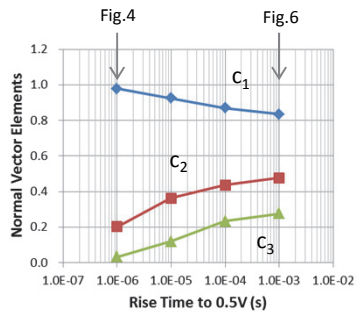

Fig.5 T_{RISE} dependence of partitioning plane direction.

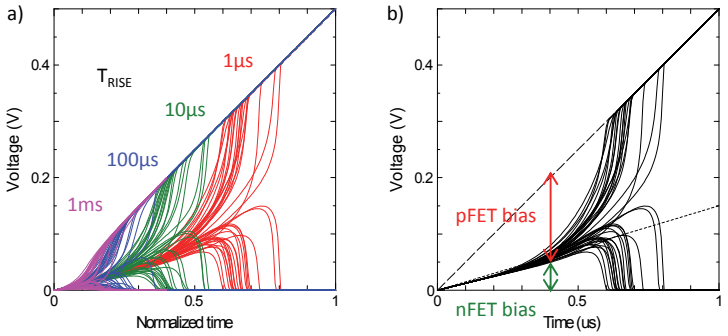

Fig.7 Node voltage waveforms during power-up. Due to stronger coupling to ground, larger voltage is applied to pFETs.

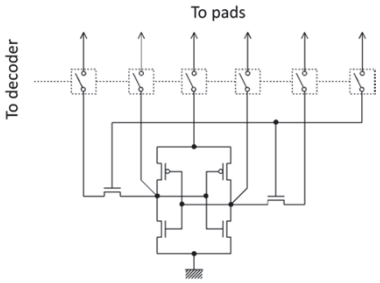

Fig.8 Unit cell of addressable cell array test structure. Both V_{TH} of individual transistors and SRAM characteristics can be measured.

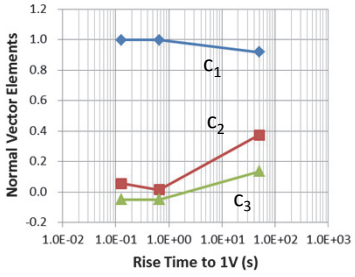

Fig.9 Measured partitioning plane direction vs T_{RISE} using test structure in Fig.8.

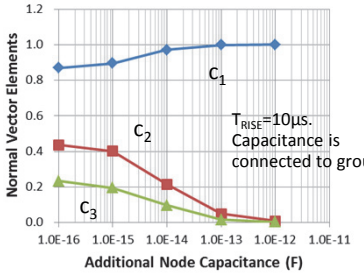

Fig.10 Partitioning plane direction vs additional node capacitance (simulated).