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Parallel Programmable Non-volatile Memory Using Normal SRAM Cells

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Abstract

A technique for using a normal SRAM array for programmable non-volatile (NV) memory is proposed. Parallel NV writing of the entire array is achieved by simply applying high-voltage stress to the power supply terminal, after storing inverted desired data in the SRAM array. Successful 2kbit NV writing is demonstrated using a device-matrix-array (DMA) TEG fabricated by 0.18μm technology.

1. Introduction

Programmable NV memory embedded in a logic chip is useful for many applications. However, using dedicated NV memory process is not cost-effective for small NV capacity. Therefore, CMOS compatible NV memory is widely studied and used. In this work, we propose a new type of programmable NV memory, which uses ordinary SRAM cells as the bit cells. Since NV data is automatically recalled into SRAM cells upon each power-up, data transfer from NV memory to SRAM becomes unnecessary. The memory operation is experimentally demonstrated and correlated with transistor characteristics using an SRAM cell array TEG.

2. Non-Volatile Writing Technique

In [1-3], a post-fabrication self-improvement technique was proposed, which improves SRAM cell stability degraded by random variation. When the power supply is turned on, bit cells prefer to be in the more stable state, corresponding to the larger opening of the so-called butterfly curves (Fig.1). That is, the cells automatically store 0 or 1 depending on the mismatch of each cell. If the power supply voltage is raised to a higher than nominal level in this situation, the butterfly curve shape of each cell will be modified so that it becomes more symmetric. This is because the pFET and nFET in the ON state (p-ON and n-ON in Fig.2a) are selectively weakened by bias-temperature (BT) stress, and the larger eye of the butterfly curves is shrunk (Fig.2b). This technique automatically alleviates the random mismatch of SRAM cells.

In this work, the same writing technique is used to realize programmable NV memory function using ordinary SRAM cells. Before the high voltage stress, instead of the automatically determined power-up data, the desired data is inverted and stored into the SRAM array. The stress modifies the butterfly curves so that the stored state will become unstable, i.e. the desired data will become more stable. If sufficient shift of the transistor characteristics is achieved such that all the butterfly curves are skewed into the intended direction, overcoming the initial mismatch, the SRAM array will recall the desired data upon power-up. That is, the SRAM array now works as a programmed NV memory. After the power-up, the array can also perform normal SRAM operation. Parallel NV writing is achieved by applying the stress voltage to multiple bits simultaneously.

3. Measurement Results

To demonstrate the above concept, a 6T-SRAM DMA-TEG [4] fabricated by a 0.18μm technology is used. The TEG is designed such that the storage nodes of each cell are directly accessible. This structure makes it possible to measure the I-V curves of individual transistors constituting the cells. Fig.3 shows the measured $|V_{THC}|$ (defined by sub-threshold constant current) distributions of the pFETs and nFETs at $|V_{ds}|$=50mV. Normal distributions are confirmed. Fig.4 shows Pelgrom plots of $|V_{THC}|$. The plots fall on straight lines passing the origin, suggesting that random dopant fluctuation (RDF) is dominant. Relatively large channel width (500nm) and length (440nm) are used in this work, since smaller variability is favorable for stable NV writing.

Fig.5a shows the distribution of the mismatch of retention noise margin (RetNM(L-R)) (Fig.1) at V_{DD}=0.6V of 2k fresh devices. RetNM(L-R) is normally distributed, and spreads in the range of about ±30mV. To write VR(High) state to all the 2k SRAM cells, RetNM should be shifted at least 30mV, so that RetNM is positive for all the bits. Recent study shows that if the node capacitance is large, as in the TEG used in this work, pFET $|V_{TH}|$ mismatch (Tp(L-R)) is more correlated with the power-up state than RetNM [5]. Therefore, Tp(L-R) distribution was also examined (Fig.5b), whose spreading range is about ±36mV.

Optimization of the stress condition is important to achieve sufficient and recovery-free V_{TH} shift, while avoiding damage to the transistors [6]. As a result of careful evaluation, NV writing stress of (5.1V, 373K, 30s) was chosen. VR=High was written to all the bits, by storing inverted VL=High and applying the stress voltage to all the cells simultaneously. Fig.6 shows (a) $|V_{THC}|$ and (b) $|V_{TH}|$ shift distributions after applying the stress. $|V_{THC}|$ variability is not changed even after applying the stress. It was also confirmed that no significant I-V curve deterioration occurs. The average $|V_{TH}|$ shift of p-ON was 33.9mV, while that of n-ON was 12.6mV. There was negligible $|V_{THC}|$ change for p-OFF and n-OFF. Fig.7 shows (a) RetNM(L-R) and (b) Tp(L-R) distributions before and after the stress. While RetNM(L-R) of all the cells after the stress were well above zero, Tp(L-R) of a few cells remained negative. Fig.8 shows histograms of RetNM(L-R) for both VR(High) and VL(High) bits at power-up (a) before and (b) after applying the stress. Fig.9 shows similar histograms for Tp(L-R). While the fresh cells exhibit nearly equal probability of VR(High) and VR(Low), all the cells recalled VR(High) after the stress. That is, NV writing of 2k cells was successful. It was also confirmed that the data stored and the shapes of the histograms were maintained after two months storing at room temperature. This shows that the recovery of BT stress was avoided.

3. Conclusion

A new concept of programmable non-volatile memory using normal SRAM cells as bit cells was proposed and demonstrated. The memory would provide new design flexibility for CMOS systems requiring a non-volatile memory function.

Acknowledgements

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References

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[5] K. Takeuchi *el al*., submitted to SSDM2016.
[6] N. E. Alias *et al*., Si Nano Workshop, p. 81, 2014.

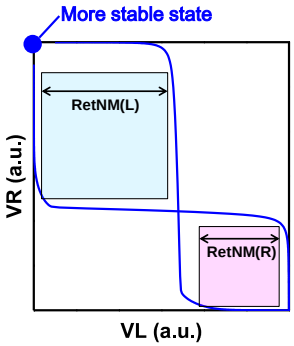

Fig.1. Example of butterfly curves in the retention condition (RetNM definition is shown). The more stable state is corresponding to the larger opening eye of the butterfly curves.

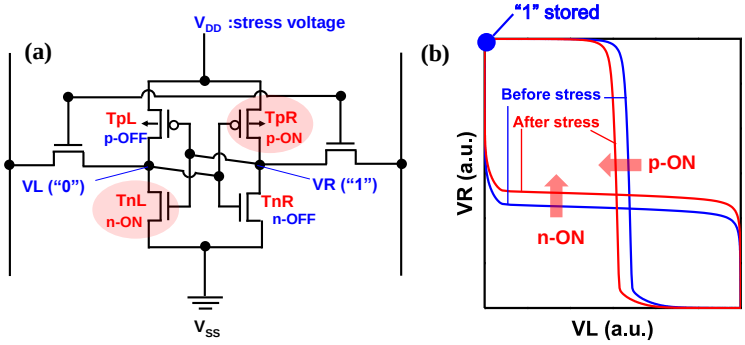

Fig.2. (a) A schematic of 6T-SRAM cell. (b) Butterfly curves before and after stress. In this example, it is assumed that VL is low and VR is high. The right pFET is p-ON and the left nFET is n-ON.

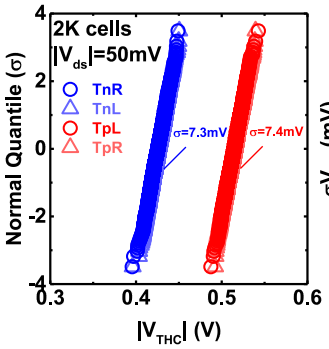

Fig.3. Measured $|V_{THC}|$ distributions of the pFETs and nFETs at $|V_{ds}|$=50mV.

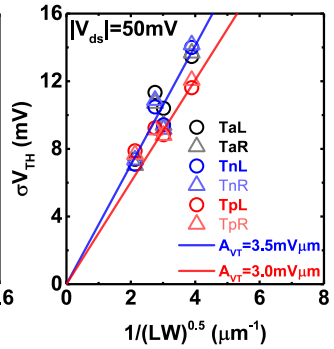

Fig.4. Pelgrom plots of $|V_{THC}|$.

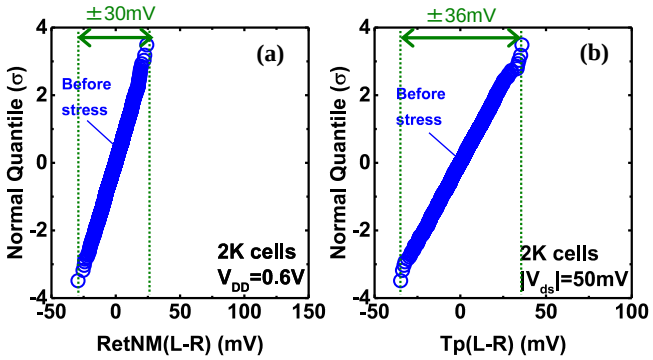

Fig.5. (a) Retention noise margin mismatch (RetNM(L-R)) at V_{DD}=0.6V and (b) pFET $|V_{TH}|$ mismatch (Tp(L-R)) distributions.

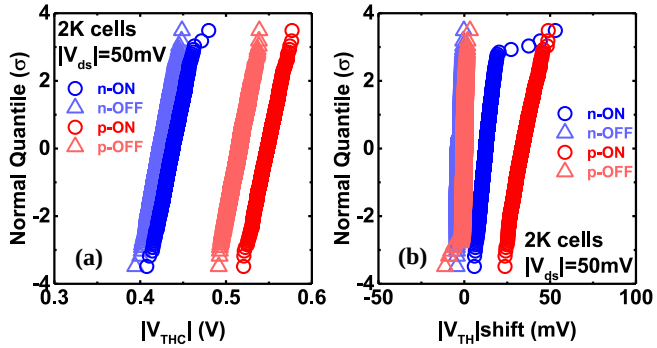

Fig.6. (a) $|V_{THC}|$ and (b) $|V_{TH}|$ shift distributions after applying stress.

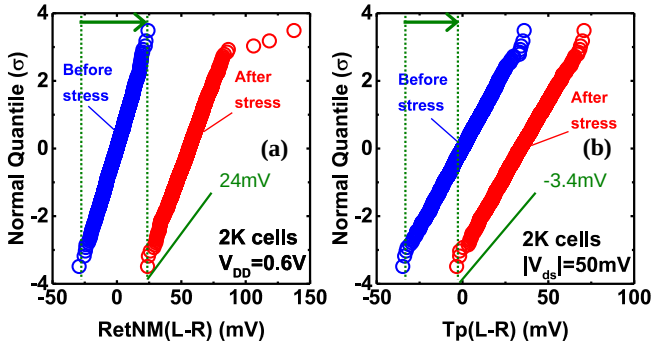

Fig.7. (a) RetNM(L-R) and (b) Tp(L-R) distributions before and after stress.

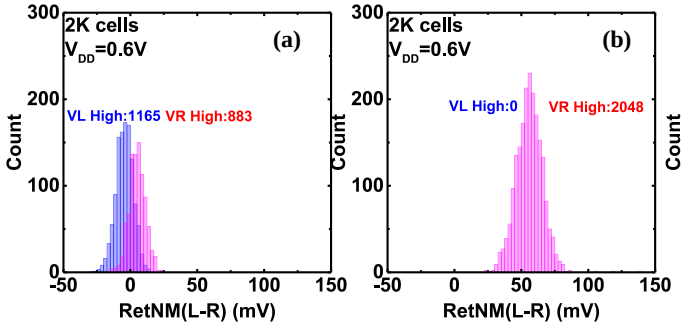

Fig.8. Histograms of RetNM(L-R) for both VR(High) and VL(High) bits at power-up (a) before and (b) after applying stress.

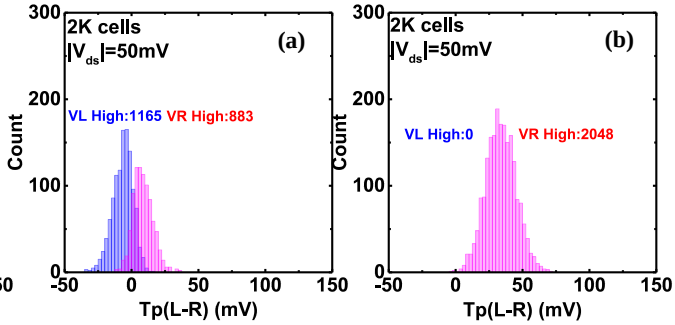

Fig.9. Histograms of Tp(L-R) for both VR(High) and VL(High) bits at power-up (a) before and (b) after applying stress.