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Gate Contact RRAM in Nano-scaled FinFET Logic Technologies

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ABSTRACT

A fully-compatible Gate Contact RRAM (GC-RRAM) cell in CMOS FinFET logic process without extra masks or processing steps has been successfully demonstrated for a high-density and low-cost logic nonvolatile memory (NVM) application. This new GC-RRAM cell composed of transition metal oxide from gate contact plug and interlayer dielectric (ILD) features low-voltage operation (<2.5V) and reset current less than 40μA, small contact area (102nmx40nm) and stable read window. Besides, as a promising embedded NVM solution, this 1T1R cell is highly scalable as technology node progressed. The new GC-RRAM cell also exhibits excellent data retention and cycling capability and is a very promising logic NVM solution for future FinFET circuits.

Introduction

As a result of its low operation voltage and high compatibility, RRAM technologies are regarded as promising solutions of logic NVMs. In recent years, various CMOS compatible RRAMs with low operation voltage, fast program speed and compact cell size have been reported and investigated by other studies [1-2]. However, these previous researches are developed on a planar CMOS logic process [3-4] and either rely on special dielectric layer or backend dielectric film for the realization of the RRAM cells [5]. As the transistor's channel mitigates from planar to 3D, changes in contact, source / drain formation and fin-shape bulk present new challenges for the development of fully-compatible NVM [6-7]. As a result, novel RRAM structures need to be investigated and developed for advanced 3D FinFET processes. In order to achieve high density and full compatibility, a new 1T1R Gate Contact RRAM is successfully implemented in pure 16nm FinFET CMOS logic process. With the Transition Metal Oxide (TMO) from the gate contact plug as a reliable resistive storage node, the Gate Contact (GC) and SiP epitaxy region serve as top and bottom electrodes, respectively, a novel RRAM cell has been proposed and demonstrated successfully in this work.

Cell Structure and Operation Principle

The proposed GCRRAM cell is fabricated by FinFET CMOS logic process with a small cell, 249nm x 346nm. The cell structure of GCRRAM is illustrated in Figure 1. As shown in the picture, the cell consists of a resistive storage film and an N-type FinFET which controls by set / reset and read of the selected cell. The resistive storage node is composed of a Ti-based Transition Metal Oxide (TMO) in the middle, the Gate Contact (GC) and N-type SiP as top and bottom electrode, respectively. By placing gate contact on top of the SiP epi-region, the gate contact etching will not completely etch through the interlayer dielectric (ILD) on top of the SiP, as illustrated in the FinFET standard logic process flow in Figure 2. This isolates the top gate contact from the bottom SiP by a thin dielectric film. The remaining ILD and contact barrier films under the W-plug form the transition metal oxide (TMO) between two electrodes and become the resistive switching film for non-volatile data storage. On the other side, the slot contact on BL side forms a regular contact on the SiP for the BL connections.

Based on the RRAM physic model proposed over the years [8-9], the low resistance path is formed by applying a large enough electric field across the TMO film, inducing the generation and/or alignment of oxygen vacancies, which form conductive filaments (CF). Reversely, a large enough reset current passing low-resistance path across TMO can disrupt the CF by the recombination of oxygen vacancies. The operation conditions of GC-RRAM are summarized in Table 1. The GC-RRAM cell are proposed to be placed into a NOR type array, see Figure 3, for obtaining a compact cell. As demonstrated in the 2 x 2 cell layout in Figure 4, following the 16nm FinFET technology design rules, cell size of 249nm x 346 nm is achieved. Gate contact sizing, which affects the contact hole etching rate, is one way to find the process window for GC-RRAMs. The cells are first screened by the initial read current, where the read current vs. gate contacts by different shapes and sizes are summarized in Figure 5. To obtain a viable RRAM device, initial read current has to be larger than 0.1nA to prevent the high forming voltage, while lower than 100nA to avoid a direct short.

GCRRAM Characteristics and Performance

It is generally believed that a conduction path is concentrated into a localized connective path consisting of CFs in the resistive storage film. The DC set / reset characteristics of the GC-RRAM cells are summarized in Figure 6, reveal that the set voltage of GC-RRAM is lower than 2.5V and reset can be achieved under a low reset current of 40μA. As demonstrated in Figure 7, a stable read current level of LRS and HRS by DC sweeps is established. Figure 8 shows the symmetric I-V characteristics under forward and reverse read directions. To optimize the LRS / HRS read current ratio, the read current ratio between LRS / HRS for V_{BL} sweep from 0 to V_{DD} in Figure 9, reveals the stable read window ~400 can be obtained once, V_{BL}>0.4V.

Higher SL voltage affects the set speed by building up higher field on sharp gate contact corners, which results in an fast program speed of 100ns, as shown in Figure 10. Increased SL voltage also enhances the reset speed (1μs) by inducing larger current as revealed by the data in Figure 11. Figure 12 shows that there is no obvious read current shift during 150℃ bake test for 120 hours. In addition, LRS / HRS read currents are monitored under a wide temperature range, showing slight positive temperature dependences in both states in Figure 13. To ensure the stable read current level during cycling, Incremental Step Pulse Programming (ISPP) algorithm is applied for both set and reset operations with pulse width of 200ns and 10μs, respectively. By setting a sequence of pulses with incremental voltage step of 50mV, the LRS / HRS read window of more than 87X can still be maintained after 10^4 ISPP cycles, as shown in Figure 14.

Conclusions

A novel FinFET Gate Contact RRAM cell, fully compatible to CMOS logic process, is proposed and successfully demonstrated in pure 16nm FinFET CMOS logic process. By the Ti-based transition metal oxide remained between gate contact plug and n+ epitaxy, GC-RRAM can be formed. Furthermore, cell superior reliability and endurance are verified by the cycling and retention test results. This high density GC-RRAM technology can be employed flexibly in advanced FinFET logic circuits.

Acknowledgements

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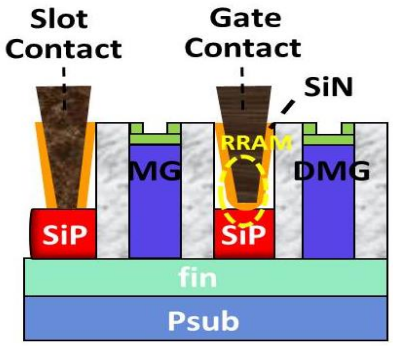

Figure 1 Schematic illustration of the Gate Contact RRAM in standard 16nm high-k metal gate FinFET CMOS process.

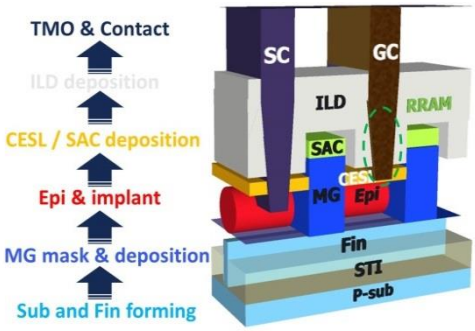

Figure 2 Standard FinFET CMOS process flow for Gate Contact RRAM. The resistive node is between SiP and Gate contact.

	Set		Reset		Read	
	Sel.	Unsel.	Sel.	Unsel.	Sel.	Unsel.
WL	0.6V	0V	1.5V	0V	0.8V	0V
BL	0V	Floating	0V	Floating	0.8V	Floating
SL	2.5V	0V	1V	0V	0V	0V

Table 1 Operation conditions of a GC-RRAM cell in a NOR-type array.

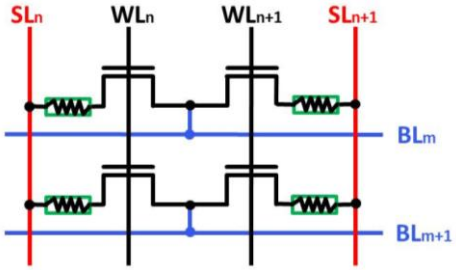

Figure 3 The 2 x 2 NOR type array with GC-RRAM cells sharing one bitline contact per two cells.

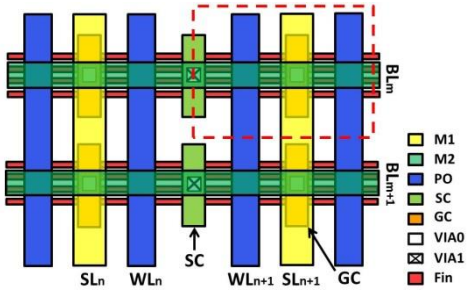

Figure 4 The 2 x 2 Cell layout of GC-RRAM. An ultra small cell is achieved in 16nm FinFET CMOS logic process.

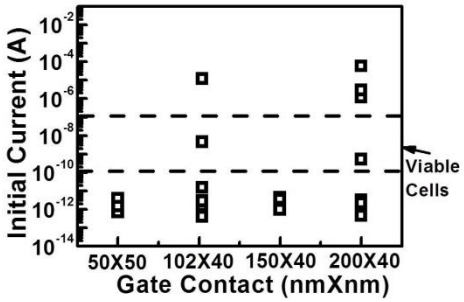

Figure 5 Initial TMO current of cells with different type of gate contact sizes, read at V_{BL} = V_{WL} = 0.8V.

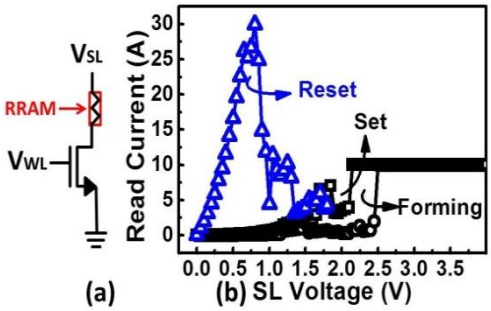

Figure 6 (a) Schematic of GC-RRAM. (b) Unipolar operation, set / forming @ V_{WL} = 0.6V and reset @ V_{WL} = 1.5V.

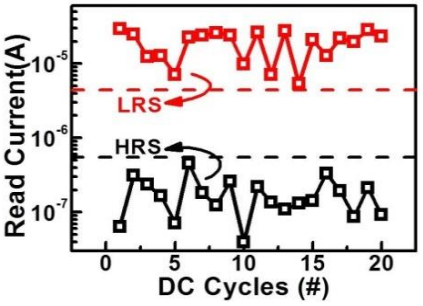

Figure 7 DC Cycling of GCRRAM with stable read window, where read condition is to set at V_{WL} = V_{BL} = 0.8V.

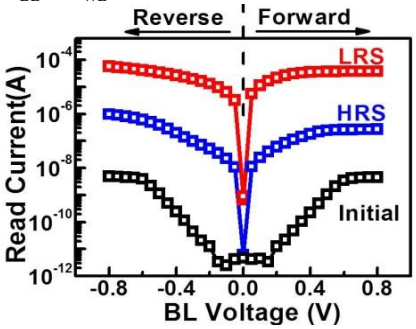

Figure 8 Characteristics under forward / reverse read. Operation suggests symmetric read behavior on Gate Contact RRAM.

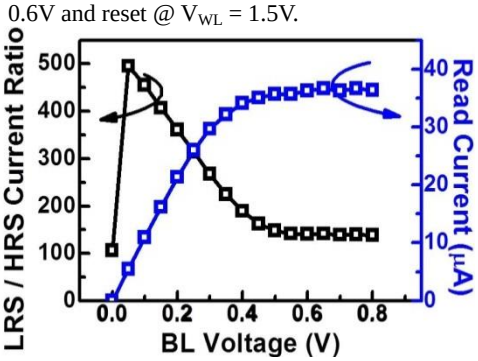

Figure 9 LRS / HRS read current ratio with different BL voltages. Stable read window are found at V_{BL} = 0.4~0.8V.

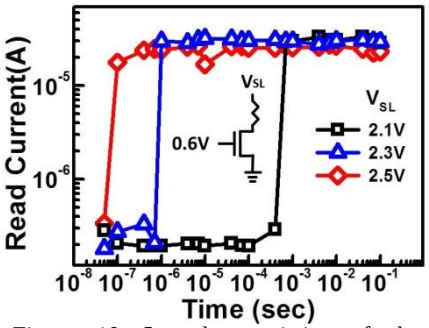

Figure 10 Set characteristics of the GC-RRAM with V_{WL} =0.6V. The set operation can be achieved within 100ns at V_{SL} = 2.5V.

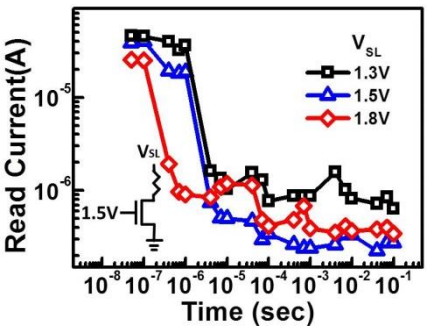

Figure 11 Reset characteristics of the GC-RRAM with V_{WL} =1.5V. The reset operation can be achieved within few micro seconds at V_{SL} = 1.8V.

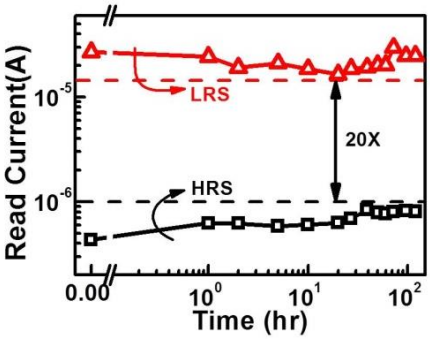

Figure 12 High temperature retention of FinFET GC-RRAM at 150℃ bake without obvious state shift.

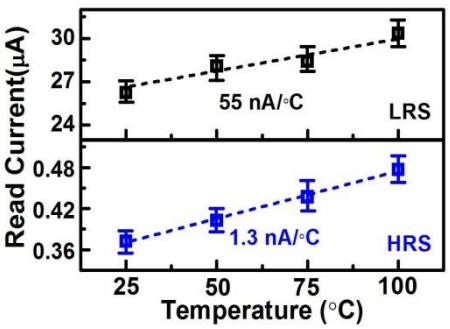

Figure 13 Two states LRS and HRS read in wide temperature range. It shows positive temperature dependence in LRS and HRS.

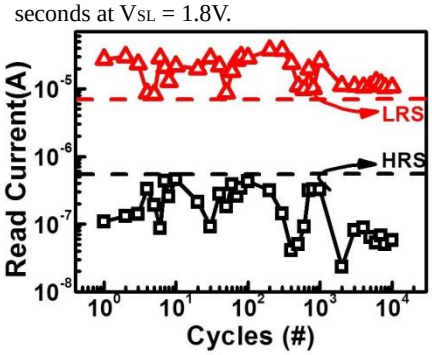

Figure 14 Endurance of ISPP algorithm with more than 10K cycles without window degradation. Set at V_{WL} = 0.6V, V_{SL} = 2.5V with 200ns and reset at V_{WL} = 1.5V, V_{SL} = 1.8V with 10μs.