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A Sidewall Electrode TiOx/TiOxNy ReRAM with Excellent Memory Window Control and Reliability Using Plasma Oxidation and a Novel Degradation-detecting Writing Algorithm

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Abstract

A TiOx/TiOxNy ReRAM with sidewall BE is demonstrated for the first time. Several interesting characteristics are observed that are very desirable for high reliability memory applications. (1) Stable RESET and SET resistance switching window even without write verification, (2) good 250°C data retention, (3) ReRAM switching instability after cycling is monitored and corrected resulting in good reliability, and (4) using only CMOS familiar materials and processes thus very manufacturing friendly. Thickness and quality of TiOx and TiOxNy are well controlled by plasma oxidation and large resistance switching window (>10X), low operation voltage and good reliability are realized.

Introduction

Transition metal oxide (TMO) resistive memory (ReRAM) is widely considered a promising next-generation memory. However, since it is based on switching between two defective states [1,2] achieving good reliability has been challenging. Ta2O5 and HfO2 based TMO ReRAM [3,4] show promising performance, but are achieved only through expensive noble metal electrode or complex buffer layers that are hard to integrate.

In this work, we report a simple ReRAM structure that can be fabricated with familiar CMOS line materials with good switching window (>10X) and excellent high temperature retention (250°C). We observed cycling instability due to the defective nature of TMO, but have designed an algorithm to monitor the cell health and achieve good reliability.

Device Structure

Figure 1 shows the TEM images for a TiN/TiOx/TiOxNy/TiN ReRAM structure using a sidewall bottom electrode (BE). The fabrication procedures are illustrated in **Fig. 2**. Although the TiN BE is physically defined by patterning, the electrical active memory area is only the top of the sidewall electrode which is converted to TiOx/TiOxNy by plasma oxidation.

Characteristics of TiOx/TiOxNy ReRAM

The influence of TiOx layer on oxidized TiOxNy is compared in **Fig. 3.** The resistance-voltage (R-V) curves are used to monitor the resistance ratio of HRS/LRS. **Fig. 3(a-b)** are for TiN/TiOxNy/TiN structure (without TiOx buffer) which shows poor HRS/LRS ratio. With 1nm TiOx layer the resistance switching ratio is >10X, as shown in **Fig. 3(c-d**). This suggests that the TiOx layer is an important O-scavenging buffer layer [5,6].

Electric field simulation results with different thicknesses of TiOx and TiOxNy are compared in **Fig. 4**. Higher E-field for thinner TiOx and TiOxNy can help reduce the operation voltage. This is experimentally confirmed in **Fig.5**. Two samples with the same TiOxNy plasma oxidation condition but different TiOx thickness of 1nm and 2nm are compared, and the thinner TiOx shows lower forming voltage. **Figure 6** shows the resistance switching distributions for the 1Mb test chip, with excellent R window stability even without write verification. Detailed device characteristics are analyzed by RESET and SET shmoo plots shown in **Fig. 7**. The switching behavior is a function of both voltage and pulse width. To achieve 10X resistance switching ratio, RESET operations require larger power and longer write pulse width than SET operation. Data retention is shown in **Fig. 8**. The memory window is maintained after 64 hours of high temperature 250°C baking.

New Write Algorithm

Cycling endurance results using conventional ISPP algorithm are shown in **Fig. 9(a)**. Instability of the SET state is observed after about 100 cycles. Strong correlation of this instability with the number of ISPP shots is show in **Fig. 9(b).** The higher number of ISPP shots corresponds to higher write voltage required to switch. However, voltage variation cannot be well controlled by ISPP and maximum voltage or current is always limited by the size of the selecting device. **Figure 10** shows the resistance vs. writing time (R-t) for ReRAM cells after 100 and 100K cycles for both SET and RESET states. There is a clear and drastic increase in write time for both SET and RESET after long cycling. This suggests that we may be able to detect the health of the cell by monitoring the write time to reach designated resistances. **Figure 11(a)** shows our new write algorithm using this degradation-aware detection scheme that includes: (1) Setup an initial write condition for initial ReRAM cells. (2) Health status of cell can be monitored by detecting if longer write pulse widths (or higher number of shots) are required. This is because degraded cells required longer writing time. (3) When degradation is detected, new write conditions are applied with multiple shots or increased pulse width without verification. By skipping the verifying steps in (3), the writing speed can be increased as compared to ISPP method. The detailed operating waveform for the new algorithm is shown in **Fig. 11(b)**. **Figure 12** compares the normal write method and the new write algorithm. Normal write without verification (single shot only) results in window closure but our new algorithm can open the resistance window again. This shows the new algorithm can prolong cycling endurance stability and solve the resistance instability issue.

Summary

A TiOx/TiOxNy ReRAM with sidewall-BE is demonstrated on a 1Mb test chip with excellent resistance switching margin and 250°C data retention. For the first time, a ReRAM degradation-aware detection method is proposed to detect cells that show cycling instability and a new program algorithm is introduced to solve resistance instability from intrinsic defect state and cycling induced cell degradation. The high temperature data retention and algorithm to ensure cycling reliability are promising for demanding automotive applications.

References

[1] Y. H. Lin et al, IEEE VLSI-TSA, 2016, to be published. [2] K.C. Hsu et al, SSDM, pp. 1168-1169, 2015. [3] S. Balatti et al, IEEE IRPS, pp.5B.3.1-5B.3.6, 2015. [4] T. Ninomiya et al, Symp. VLSI Tech., pp.73-74, 2012. [5] H.Y. Lee et al, IEEE IEDM Tech. Dig., pp. 1-4, 2008. [6] B.Govoreanu et al, IEEE IEDM Tech. Dig., pp. 31.6.1 - 31.6.4, 2011.

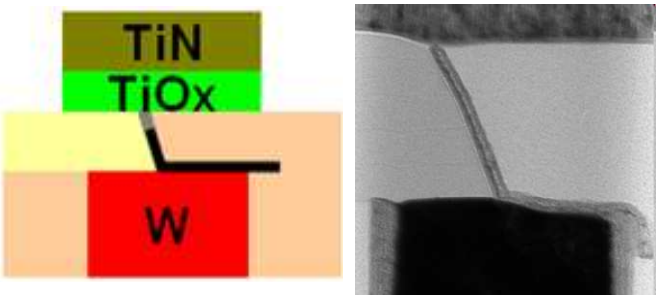

Fig. 1 Cross-sectional TEM images of the side-wall TiOx/TiOxNy ReRAM structure fabricated on W plug.

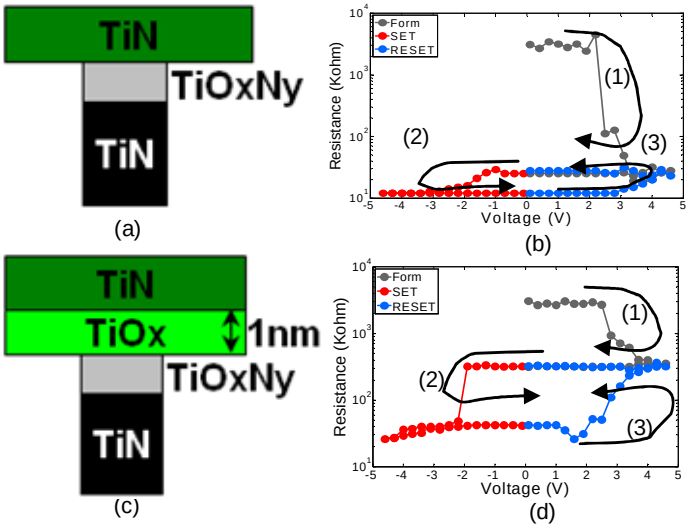

Fig. 3 Two different sidewall ReRAM structures are fabricated. (a-b) Structure without TiOx layer and the corresponding measured R-V curve. (c-d) Structure with 1nm TiOx layer and measured R-V curve. Device without the TiOx layer shows poor switching. Optimizing the TiOx/TiOxNy structure is key to achieve >10X switching window.

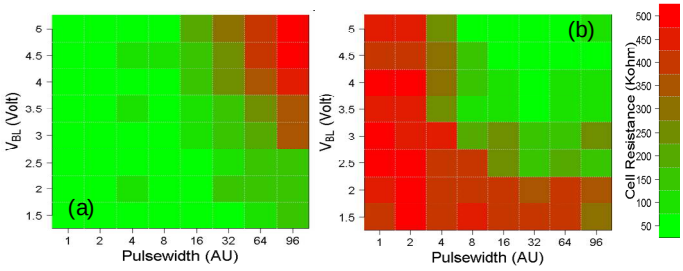

Fig. 7 Shmoo plots for (a) RESET and (b) SET operations. The resistance is a function of voltage and pulse width for both SET and RESET operations.

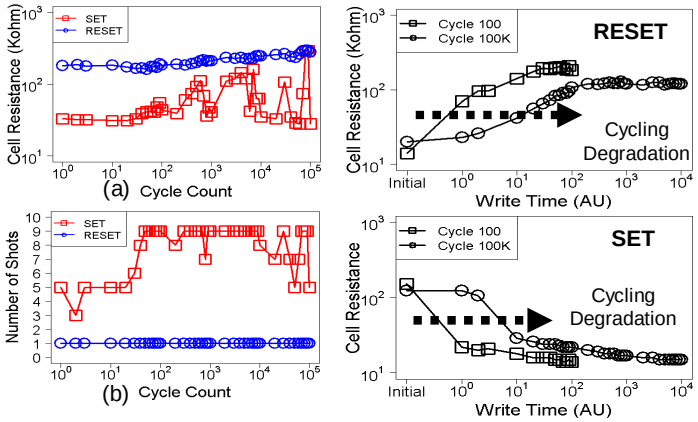

Fig. 9 Cycling behavior. (a) SET becomes unstable after ~ 100 cycles. (b) Number of shots increase concomitantly with cycling instability.

Fig. 10 Cycling degradation can be detected by increase in write time.

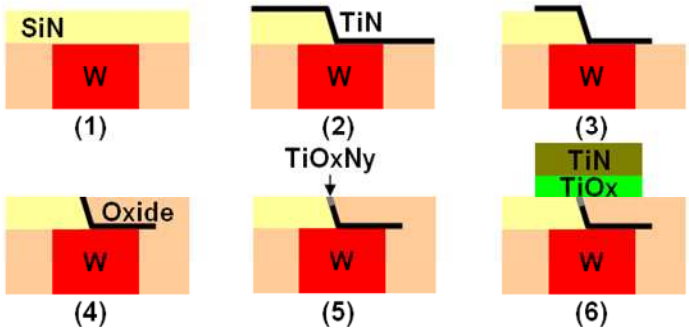

Fig. 2 Process flow for side-wall TiOx/TiOxNy ReRAM. (1) SiN deposition after W CMP, (2) trench formation and TiN deposition, (3) bottom TiN definition, (4) planarization, (5) plasma oxidation to form TiOxNy, and (6) formation of TiOx and TiN top electrode.

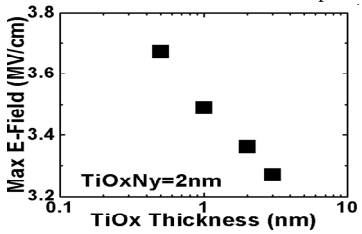

Fig.4 Simulated electric field distribution (at middle of the TiOx/TiOxNy interface) vs. different TiOx thicknesses.

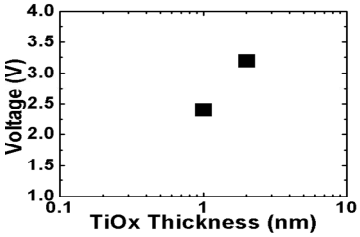

Fig.5 Forming voltage measured for devices with various TiOx thickness. Results are consistent with simulation shown in Fig. 5.

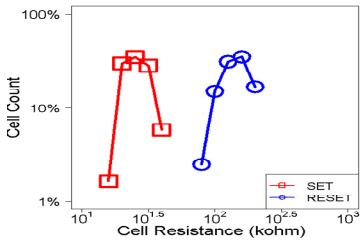

Fig. 8 Good data retention behavior after 64hr 250˚C baking.

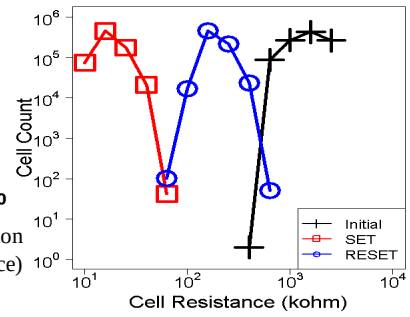

Fig. 6 Resistance distributions for initial R, RESET and SET states without write verifying procedure. Good RESET/SET R distribution is demonstrated after single write pulse without verification.

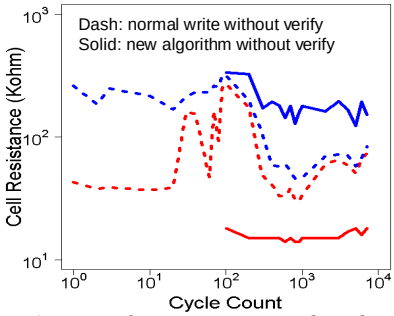

Fig. 12 The new writing algorithm achieves good resistance distribution window without write verifying procedure.

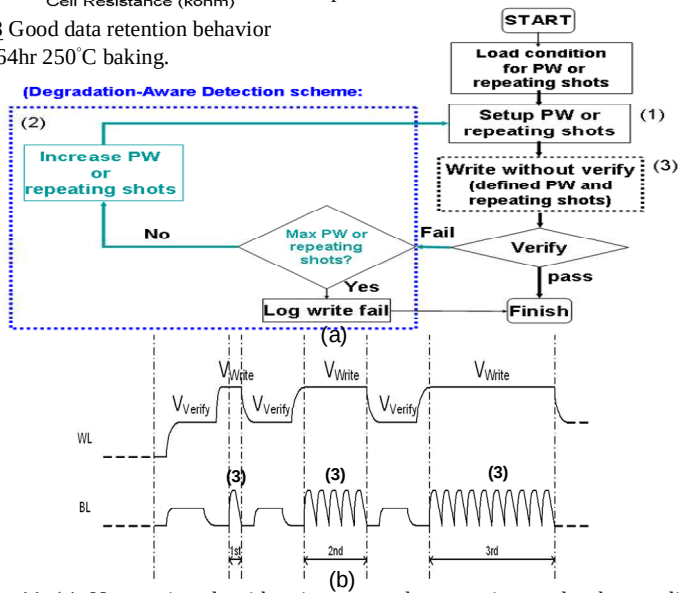

Fig. 11 (a) New write algorithm is proposed to monitor and solve cycling degradation. Increases in pulse width or write shots serve as cell health monitor and additional write without verify is called to correct the problem. (b) Operating waveform for the new write algorithm.