Multi-level operation of a high-speed, low power topological switching random-access memory (TRAM) based on a Ge deficient Ge_xTe/Sb₂Te₃ superlattice

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Abstract

We used first principles simulations to confirm the high-speed operation and low power switching of a topological switching random-access memory (TRAM) based on a Ge deficient Ge_xTe/Sb_2Te_3 superlattice. We also demonstrated that multi-level operation is possible for TRAMs utilizing GeTe/Sb₂Te₃ superlattices. Furthermore, simulation showed that the LRS resistance of GeTe/Sb₂Te₃ superlattice TRAMs can be tuned by changing the number of injected holes. In experiments, high-speed, low power switching and multi-level operation have indeed been observed.

Introduction

A new type of phase change RAM (PRAM), known as a topological switching RAM (TRAM), for use as a high-speed, low power non-volatile memory has been examined [1]. The HRS and LRS of a TRAM can be switched by the movement of Ge atoms (Fig.1(a)) It has been shown, using first principles calculations, that the movement of atoms in TRAMs increases with carrier injection [2]. Recently, it has been found that TRAMs based on Ge deficient Ge, Te/Sb₂Te₃ superlattices with x<<1 have higher speed operation and lower switching power than stoichiometric GeTe/Sb2Te3 superlattice TRAMs [3]. However, the conventional theoretical models for TRAMs [4] cannot explain the improvement in switching characteristics of Ge deficient TRAMs. In this paper, we investigate the on-off switching properties of a Ge_xTe/Sb₂Te₃ superlattice TRAM using first principles molecular dynamics simulation in which heating and carrier injection can be separately examined. Our simulations show that high-speed and low power switching operations can be realized in Ge deficient TRAMs. Ge atoms at the interfaces between the GeTe and Sb₂Te₃ open the conduction paths (Fig.1(b), Fig.2(b)). Thus, the presence of Ge atoms at these interfaces determines the resistance state (Fig.2(a),(b)). (If Ge atoms are present at the interfaces, it is LRS.) Note that HRS and LRS can be modeled by an equivalent circuit (Fig.2). Moreover, we confirmed that Ge vacancies in the GeTe layer enhance the Ge mobility, giving rise to low power and high-speed memory operations of Ge deficient TRAMs. We also showed that the LRS resistance can be controlled by changing the number of injected holes during the set operation, indicating the possibility of multi-level operation of TRAMs. Multi-level LRSs of a TRAM have indeed been observed experimentally [5].

Simulation model and method

We prepared a stoichiometric GeTe/Sb₂Te₃ superlattice and a Ge deficient $Ge_{0.44}$ Te/Sb₂Te₃ superlattice. The atomic and electrical structures were obtained using VASP [6], which is based on density functional theory. On-off switching was simulated by carrier injection during the set and reset operations using first principles molecular dynamics. The heat was simulated by giving the atoms kinetic energy, whereas carrier injection was simulated by changing the number of electrons in the system. Thus, heating and carrier injection was simulated by Joule heating and hole injection. On the other hand, the reset operation was simulated by Joule heating alone (**Fig. 3**). Moreover, the Joule heat and the number of holes injected during the set and reset operations were varied (**Fig. 3**).

HRS and LRS structures of a Ge_xTe/Sb_2Te_3 superlattice TRAM obtained using first principles molecular dynamics

After heating, all the Ge atoms in the Ge_xTe/Sb_2Te_3 superlattice TRAM are located in the central GeTe layer (**Fig.4(a)**,(**c**)). These structures correspond to HRS. On the other hand, after injecting holes and heating, some Ge atoms move to the GeTe/Sb₂Te₃

interfaces (**Fig.4(b)**,(**d**)). These structures correspond to LRS. This switching model is a natural expansion of Tominaga's model (**Fig.1(a**)) [4]. Moreover, the durability of this mechanism in program/erase cycles is excellent. This is because HRS-LRS switching can be realized by the movement of Ge between the center of the GeTe layer to interfacial positions between the GeTe and Sb₂Te₃. In other words, only the vertical position of the Ge is crucial in switching and the horizontal position is unimportant. In fact, the endurance in program/erase cycles has been reported as being more than 10^7 cycles [3].

High-speed and low power operation of Ge deficient TRAMs

We compared the HRS-LRS switching properties of stoichiometric GeTe/Sb₂Te₃ and Ge deficient $Ge_{0.44}Te/Sb_2Te_3$ TRAMs. As shown in **Fig.5**, Ge deficient TRAMs switch successfully with both 20.8kJ/mol and 8.3kJ/mol heating. However, switching in stoichiometric ones failed in the case of 8.3kJ/mol heating. Thus, Ge deficient TRAMs can operate with lower switching power. Moreover, the diffusion coefficient of Ge in Ge deficient TRAMs is larger than in stoichiometric TRAMs (**Fig.6**), indicating that they can operate at high speed. In fact, they can operate with higher speed and lower power compared with stoichiometric TRAMs. These results are consistent with experimental reports (**Fig.7**). The set voltage of the Ge deficient TRAM is 0.5V (**Fig.7(a)**), 40% less than the stoichiometric one. Moreover, the Ge deficient TRAM can switch with a 5ns pulse, which is much faster than a conventional PRAM (**Fig.7(b**)).

The possibility of multi-level-cell operation for a GeTe/Sb₂Te₃ superlattice TRAM

As shown in the equivalent circuit model (Fig.2), the LRS resistance can be controlled by changing the number of Ge atoms at the interfaces between the GeTe and Sb_2Te_3 (Fig.8). This means that multi-level operation is possible if we can change the number of Ge atoms at these interfaces. We used first principles molecular dynamics simulations to control the LRS resistance by changing the number of injected holes in the TRAM by applying 20.8kJ/mol of heat. The simulated results show that the number of Ge atoms at the interfaces as the number of injected holes increases (Fig.8), suggesting that the LRS resistance can be controlled by changing the number of injected holes. Multi-level LRSs have indeed been observed experimentally (Fig.9) [5]. Accordingly, with GeTe/Sb₂Te₃ superlattice TRAMs multi-level memory operation can be achieved by changing the number of injected carriers during the set operation.

Conclusion

We examined the memory properties of Ge_xTe/Sb_2Te_3 superlattice TRAMs. $Ge_{0.44}Te/Sb_2Te_3$ superlattice TRAMs operate with higher speed and lower switching power than stoichiometric $GeTe/Sb_2Te_3$ superlattice TRAMs. Moreover, multi-level memory operation can be achieved by changing the number of injected carriers.

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TRAM. (b) Ge conduction path models for HRS and LRS in a TRAM. The presence of Ge atoms at the GeTe/Sb₂Te₃ interfaces distinguishes HRS from LRS.

Fig. 2 Schematic illustration of the Ge conduction path model and equivalent circuits. LRS is identified by the presence of Ge atoms at the GeTe/Sb₂Te₃ interfaces.

Fig 3 On-off switching is simulated by carrier injection and heating using first principles molecular dynamics.

-0.7 ~ +0.7



Fig. 4 Simulated HRS and LRS structures of Ge_xTe/Sb₂Te₃ (x=1, 0.44). HRS (a) and LRS (b) structures of a stoichiometric GeTe/Sb₂Te₃ superlattice and HRS(c) and LRS(d) structures of a Ge deficient Ge_{0.44}Te/Sb₂Te₃ superlattice. The HRS structures ((a) and (c)) were obtained by injecting holes and heating. The LRS structures ((b) and (d)) were obtained by heating only. In the HRS structures, all the Ge atoms are located in the central GeTe layer, whereas in the LRS structures some of the Ge atoms are located at the GeTe/Sb₂Te₃ interfaces. These results suggest that HRS changes into LRS by hole injection and Joule heating and that LRS changes to HRS by Joule heating alone.



Fig. 5 Results of on-off switching simulation. The Ge deficient TRAM switches successfully with both 20.8kJ/mol and 8.3kJ/mol heating. However, the stoichiometric TRAM fails to switch in the case of 8.3kJ/mol heating. These results indicate that the switching power of the Ge deficient TRAM is lower than the stoichiometric TRAM.



diffusion coefficient in the Ge deficient TRAM is larger than the stoichiometric TRAM, resulting in high-speed switching of the Ge deficient TRAM.



Fig. 7 R-V curves for a Ge_xTe/Sb₂Te₃ TRAM. (a) x dependence of the set operation. (b) Nanosecond switching characteristics. The value of the set voltage for the Ge deficient TRAM is 0.5V. The Ge deficient TRAM can switch with a 5ns pulse.



1E+8 1E+71E+6 LRS3 1E+5 LRS2 1E+4 LRS 1E+3 0.5 0.6 0.7 0.8 0.9 1 1.1 Voltage [V]

Fig. 8 Three simulated LRS structures of a stoichiometric GeTe/Sb,Te₃ superlattice that were obtained by 20.8 kJ/mol heating. Structures obtained after (a) 0.5, (b) 0.32 and (c) 0.21 e/atom hole injection. The resistance value decreases as the number of injected holes increases. These results suggest that multi-level operation is possible by changing the number of injected holes.

Fig. 9 R-V curves of a TRAM for the set operation. Multi-level LRSs can indeed be observed experimentally (Reference [5]).