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Combination of Volatile and Non-volatile Functions in A Single Memory Cell with Independent Asymmetric Dual-Gate Structure

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Abstract

A single memory cell which combines volatile and non-volatile functions has been demonstrated with an independent asymmetric dual-gate structure. Owing to the second gate whose dielectric is composed of oxide/nitride/oxide layers, floating body effect is observed even on a fully depleted silicon-on-insulator (FDSOI) device and a non-volatile memory function is measured. In addition, 1T-DRAM operation characteristics depending on non-volatile memory state are evaluated and analyzed. These results indicate that the proposed device is a promising candidate for high-density embedded memory applications.

1. Introduction

Integration of volatile and non-volatile memory functions in a single device has attracted much attention for embedded systems [1-2]. However, most of the memory devices utilizing floating body effects should be implemented on a partially depleted silicon-on-insulator (PDSOI) substrate for the excess hole storage. This is a limitation in scaling down gate length and floating body thickness, because retention properties of floating body suffer from short channel effects such as drain-induced barrier lowering (DIBL) and PDSOI structure cannot effectively suppress these problems [3-5].

In this work, a single memory cell having both volatile and non-volatile functions is demonstrated with an independent asymmetric dual-gate and a thin, fully depleted body. The volatile memory (VM) can be obtained even in a fully depleted body thanks to the field effect of trapped charges in the nitride layer and the nitride layer allows the non-volatile memory (NVM) in the device at the same time. The reliability characteristics are also discussed and high speed VM operations are confirmed.

2. Results and Discussion

Device Concepts

A single memory cell with both volatile and non-volatile functions is fabricated. The first gate (G1) dielectric and the second gate (G2) dielectric are composed of oxide layer and oxide/nitride/oxide layers, respectively. This gives both VM and NVM functions to the device because electrons can be trapped in the nitride layer and the trapped electrons allow an electrically induced floating body effect even on a fully depleted body. Figure 1 shows the cross-sectional HR-TEM image of the fabricated device. The transfer curves of the G1 and the G2 have different subthreshold characteristics as shown in Fig. 2, which confirms that two gates are electrically separated. The fabrication details are described elsewhere [6-7].

Non-volatile Memory Function

Figure 3 shows the transfer curve of the G2 after program and erase operations made by applying the G2 voltage (V_{G2}) of 15 V for 100 μs and -15 V for 1 ms, respectively. The threshold voltage (V_T) window is 4.5 V which is large enough to distinguish two states. The retention properties of the NVM at 85 °C are measured as shown in Fig. 4. The accelerated charge loss at 85 °C was extracted to be 48% after 10 years.

Volatile Memory Function

Figure 5 shows the output characteristics for different states of the NVM. The kink effects are not observed at the erased state due to the lack of excess hole storage room resulting from a fully depleted body. On the contrary, there is a kink effect at the programmed state because the trapped electrons in the nitride layer evoke an electrically induced floating body effect. It means that the VM function can be obtained when electrons are trapped in the nitride layer.

Figure 6 shows transient source current characteristics of the VM at the erased state and the programmed state. The bias conditions of the write "1" and "0" states are $V_{G1} = V_D$ = 1.5 V and V_{G1}= 1.5V, V_D = -1.5 V, respectively. The sensing margin, defined as the source current difference at the read condition (V_{G1} = 1.5 V, V_D = 0.5 V), is negligible at the erased state but clear at the programmed state owing to the high storage capacity of positive charges in the body. The read retention properties are also improved at the programmed state as shown in Fig. 7. The read retention time is 30 μs at the erased state while over 0.1 s at the programmed state. It is suggested that the sensing margin and retention characteristics can be also promoted by trapping charges without additional biasing on the G2.

Finally, the soft programming characteristics of the NVM are evaluated under the dc stress ($V_{G1} = V_D$ = 1.5 V) which is the write "1" condition of the VM as shown in Fig. 8. It is found that V_T of the erased and programmed states is nearly unchanged over 10^4 s. This is because impact ionization during the VM operation occurs near the G1 and the nitride layer is placed apart by the channel thickness. Figure 9 shows the flow of the device operation. The initialization has to be preceded before using the device as the VM cell.

3. Conclusions

A single memory cell having both VM and NVM functions with independent asymmetric gates is demonstrated. The NVM resulting from the G2 stack is measured and analyzed. The device has floating body effects despite a fully depleted body thanks to the trapped negative charges in the nitride layer because they allow an electrically induced floating body effect. Since two gates are placed apart by the channel thickness, the NVM has immunity to soft programming in the VM operations. These findings lead us to conclude that it is a promising candidate for ultra-high-density applications.

Acknowledgements

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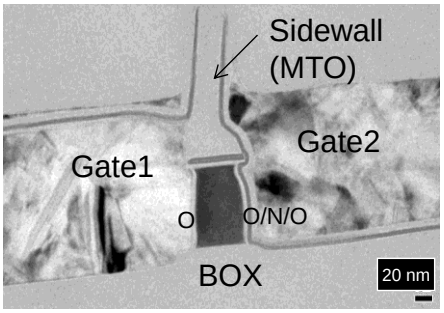

Fig. 1 Cross-sectional HR-TEM image of the fabricated device

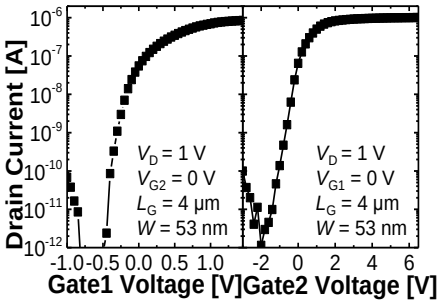

Fig. 2 Transfer curves of the G1 and G2 with different subthreshold characteristics.

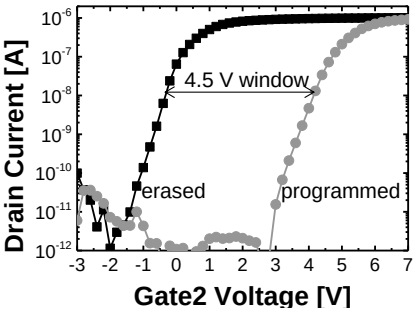

Fig. 3 V_T window after program/erase operation

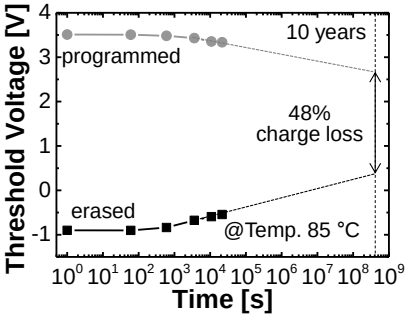

Fig. 4 Retention properties of the NVM at 85 °C.

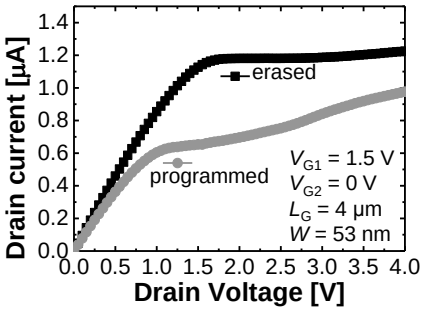

Fig. 5 Output curves at the erased state and the programmed state of the nitride layer.

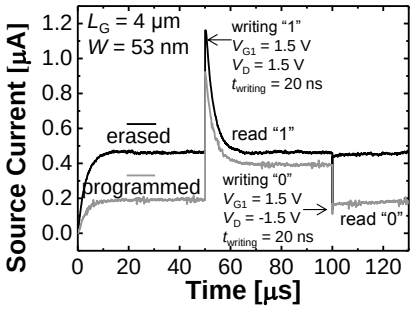

Fig. 6 Transient source current characteristics of the VM function.

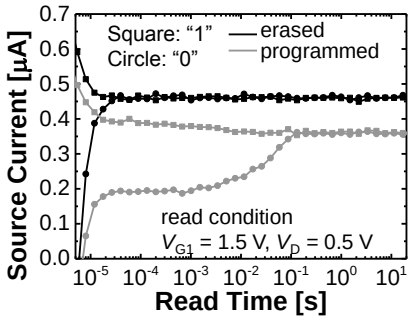

Fig. 7 Read retention properties of two states of the NVM.

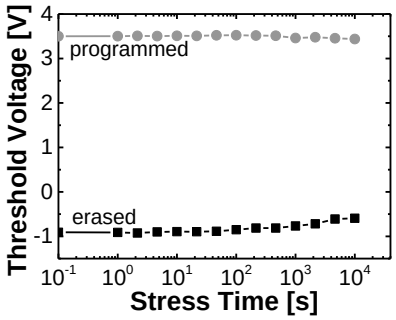

Fig. 8 Soft programming issues under the dc stress (V_{G1} = V_D = 1.5 V).

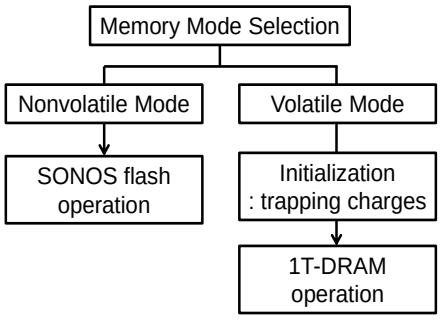

Fig. 9 Operational flow of the proposed device.