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3.3 V write-voltage Ir/$Ca_{0.2}Sr_{0.8}Bi_2Ta_2O_9$/$HfO_2$/Si ferroelectric-gate field-effect transistors with 10^9 endurance and good retention

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Abstract

3.3 V operations of FeFETs were demonstrated. The gate stack was Ir/$Ca_{0.2}Sr_{0.8}Bi_2Ta_2O_9$ (CSBT)/HfO_2/Si where CSBT was 135 nm thick. After 780 ºC poly-crystallization annealing for CSBT, an SiO_2-like interfacial layer formed between HfO_2 and Si was as thin as 2.6 nm using N_2-dominant gas of 1000 sccm N_2 with 0.5 sccm O_2 added. The Ir gate showed good adhesion on the CSBT during the 780 ºC annealing in the N_2-dominant ambient. The novel FeFET operated at V_g = ±3.3 V indicated a large 0.59 V memory window, 10^9 cycles endurance and long retention measured for 10^5 s.

1. Introduction

Metal/ferroelectric/insulator/semiconductor (MFIS) type ferroelectric-gate field-effect transistors (FeFETs) have been attracted considerable attention owing to their potentially-scalable memory cells, very low power dissipation, and non-destructive read operation [1]. Since a first successful FeFET with high endurance and long retention was reported [2], we have developed FeFET integrated circuits [3,4] and single-cell downsizing [5]. The circuits were non-volatile logic [3] and Fe-NAND flash memories [4], for example. The recent downsizing work demonstrated a 100 nm metal-gate FeFET with high performance [5]. The gate stacks of our FeFETs were early Pt/$SrBi_2Ta_2O_9$(SBT)/$(HfO_2)_{0.75}(Al_2O_3)_{0.25}$(Hf-Al-O)/Si, then Pt/$Ca_xSr_{1-x}Bi_2Ta_2O_9$(CSBT)/Hf-Al-O/Si and recently Pt/CSBT/HfO_2/Si. The CSBT was more effective for widening memory window (V_w) than the SBT [6]. The V_w was a threshold-voltage (V_{th}) difference in a drain-current *vs* gate-voltage (I_d-V_g) curve of the FeFET. The V_{th} in this study was defined as the V_g at $I_d = 10^{-8}$ A/μm. We selected Bi-layered-perovskite ferroelectric materials of the SBT and CSBT with expecting the high endurance nature in FeFETs. However, the SBT and CSBT required about 800 ºC annealing for exhibiting their ferroelectricity. During the poly-crystallization annealing in O_2 ambient, a 3.4 nm-thick or more SiO_2-like interfacial layer (IL) was inevitably grown on the Si surface [6, 7]. Such a thick low-*k* IL was an obstacle to reducing V_g for writing the FeFET less than 5 V. In this work, we report 3.3 V write operations of FeFETs by reducing the IL thickness to 2.6 nm.

2. Experimental

For realizing the thin IL, we started from an idea that the annealing process had two aspects: one was crystallizing the (C)SBT from the amorphous precursors by sufficiently-high temperature. The other was complementing the oxidization of the (C)SBT by an enough oxygen supply. In this study, our CSBT was deposited by pulsed laser deposition (PLD) using a ceramic target of Ca-Sr-Bi-Ta-O. The precursor made by the PLD was expected to include sufficient oxygen before the annealing. Therefore we tried the FeFET annealing in N_2-dominant ambient instead of the conventional pure O_2. Many FeFETs were prepared by systematically varying the gas-flow ratio of small-amount O_2 to be mixed into N_2. In the FeFET preparation processes, we found that Pt films peeled off every when the Pt/CSBT/HfO_2/Si stacks were annealed in the N_2-dominant ambient at about 780 ºC. Among several candidates as the substitute metal for the Pt, Ir showed good properties as a gate electrode in the Ir/CSBT/HfO_2/Si FeFETs which underwent the annealing in N_2-dominant ambient at 780 ºC.

2-1. Optimizing N_2:O_2 gas-flow ratio

Figure 1 shows memory windows measured at V_g = ±3.3 V of many Ir/CSBT(x = 0.2)/HfO_2/Si FeFETs. The thicknesses were 75 nm Ir, 135 nm CSBT, and 4 nm HfO_2 common to the all FeFETs. The FeFETs had non-self-aligned gates. The gate length (L) was L = 10 μm. They were fabricated by annealing in 1atm N_2-and-O_2 mixed gas at 780 ºC for 30 min. An infrared-gold-image furnace (ULVAC SINKU-RIKO) was modified and used. The quartz chamber was evacuated to about 2 Pa by a dry-scroll vacuum pump every time before filling the gas to 1atm. The gas was 1000 sccm N_2 with a little O_2 added which were varied from 0.1 to 3 sccm. As shown in Fig. 1, the largest memory windows was V_w = 0.59 V which was obtained at the O_2 flow of 0.5 sccm. Note that the pure N_2 annealing was not suitable for enlarging V_w probably because some oxygen was required for CSBT poly-crystallization during the annealing. The V_w = 0.59 V at the 3.3 V write voltage was significantly large in spite of using such a thin CSBT as 135 nm. We could see how large the V_w was in comparison with five reference FeFETs (Refs. A-E) prepared by the different annealing gas conditions as summarized in Table.1. The V_{amp} was defined as the V_g amplitude. All the reference FeFETs in Table.1 also had L = 10 μm non-self-aligned gates. Refs. A and B were annealed in N_2 dominant gas with more O_2 and with no O_2 mixtures. The both showed much less memory windows at V_g = ±3.3 V. The other FeFETs of Refs. C, D and E had Pt gates. Therefore, they were annealed in pure O_2 for avoiding the Pt peeling off. All of Refs. C, D and E showed smaller V_ws than the FeFET developed in this work. Note that memory windows of Refs. C, D and E were measured at V_g = 1 ± 3.3 V. The 1 V was corresponding to a flat-band voltage shift of the MFIS which was adjustable by the Si channel dose. Memory windows of Refs. C, D and E became small as the CSBT thickness was reduced from 200 nm to 120 nm. The largest V_w = 0.37 V of Ref. C was still smaller than the FeFET in this work. The large V_w of this work in comparison with the Refs.A-E was explained by a cross-sectional TEM images in Figs.2(a) and (b). Figure 2(a)

indicated that the IL of this work was as thin as 2.6 nm. The FeFET was annealed at 780 ºC in the optimum ambient of 1000 sccm N_2 with 0.5 sccm O_2 added as described in Table. 1. On the other hand, a reference in Fig. 2 (b) showed 3.4 nm-thick IL. The reference was a Pt/CSBT(x = 0.1)/Hf-Al-O/Si FeFETs with the 200 nm-thick CSBT and the 7 nm-thick Hf-Al-O. It was annealed at 778 ºC in pure O_2. The IL thicknesses in FeFETs would not be decreased by annealing in O_2 dominant ambient.

2-2. Electrical properties

We investigated endurance and retention of the novel FeFET with V_w = 0.59 V at V_{amp} = 3.3 V. It was the Ir/CSBT(x = 0.2)/HfO_2/Si FeFET annealed at 780 ºC in the optimum ambient of 1000 sccm N_2 with 0.5 sccm O_2 added. An endurance cycle was a pair of +3.3 V and -3.3 V pulses with a 20 μs period as indicated in the inset of Fig. 3 (a). As indicated in Fig. 3 (a), the FeFET maintained the V_{th} difference of about $V_{th}e - V_{th}p$ = 0.55 V up to 10^9 cycles. The $V_{th}e$ and $V_{th}p$ were the erase- and program-V_{th} values which were extracted from an I_d-V_g curve measured at every accumulated endurance cycle as shown in Fig. 3(b). Figure 3(b) indicated that the I_d-V_g curves drawn at the endurance cycles of 10^3 and 10^9 were almost the same. V_{th} retentions of the FeFET were measured for 10^5 s as shown in Fig. 4. After a V_g = -3.3 V erase-pulse or a V_g = +3.3 V program-pulse was applied for 0.1 s, all terminals of the FeFET, gate, drain, source and substrate, were hold at $V_g = V_d = V_s = V_{sub}$ = 0 V. At every marker in the retention curves in Fig. 4, I_d-V_g was measured by narrow-scanning V_g from 1.0 V to 0 V with V_d = 0.1 V for nondestructive reading $V_{th}e$ or $V_{th}p$. The FeFET retained the V_{th} difference of at least $V_{th}e - V_{th}p$ = 0.3 V for 10^5 s. Similarly, after a V_g = -2.9 V erase-pulse or a V_g = +2.9 V program-pulse was applied for 0.1 s, we held $V_g = V_d = V_s = V_{sub}$ = 0 V. At every marker in the corresponding curves in Fig. 4, I_d-V_g curve was measured by scanning V_g from 0.9 V to 0 V with V_d = 0.1 V for nondestructive reading of the $V_{th}e$ or $V_{th}p$. The FeFET retained the V_{th} difference of at least $V_{th}e - V_{th}p$ = 0.2 V for 10^5 s. Extrapolation lines in Fig. 4 suggested that the FeFET had a potential of ten-years retention by the less write voltages than 3.3 V.

3. Summary

Low-voltage 3.3 V operations of an Ir/CSBT(x = 0.2)/HfO_2/Si FeFET was demonstrated for the first time. Large 0.59 V static V_w, high 10^9 cycles-endurances and 10^5s-long good retentions of the FeFET were confirmed by the 3.3 V writing. Poly-crystallization annealing in N_2-dominant gas of 1000 sccm N_2 with 0.5 sccm O_2 added was the key process both for obtaining good CSBT ferroelectricity and for realizing a thin 2.6 nm IL.

Table I This work *vs* reference FeFETs.

	V_w at V_{amp}=3.3V	Stacked materials on Si and the thicknesses	Annealing	
			Gas flow	Temp.
This work	**0.59 V**	**Ir/CSBT(x=0.2)/HfO_2 75 nm/135 nm/4 nm**	**N_2 : O_2 = 1000 : 0.5**	780 ºC
Ref. A	0.29 V	75 nm/135 nm/5 nm	1000 : 10	
Ref. B	0.18 V	75 nm/135 nm/5 nm	pure N_2	
Ref. C	0.37 V	Pt/CSBT(x=0.2)/Hf-Al-O 200 nm/200 nm/7 nm	pure O_2	778 ºC
Ref. D	0.25 V	200 nm/160 nm/7 nm		800 ºC
Ref. E	0.22 V	200 nm/120 nm/7 nm		

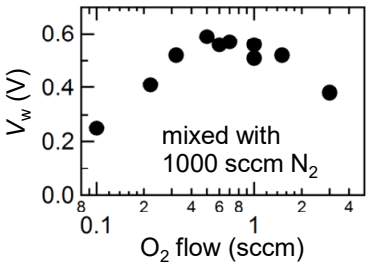

Fig. 1 Memory windows measured at V_g = ±3.3 V of Ir/CSBT(x = 0.2)/HfO_2/Si FeFETs.

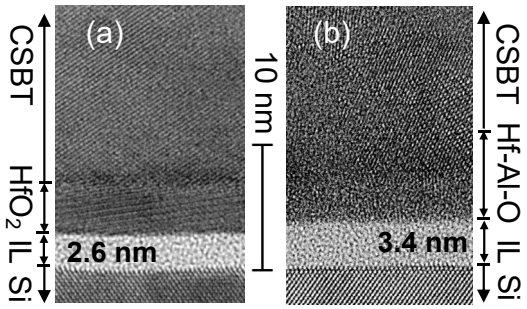

Fig. 2 Cross-sectional TEM images of this work (a) and a reference Pt/CSBT(x = 0.1)/Hf-Al-O/Si FeFET (b).

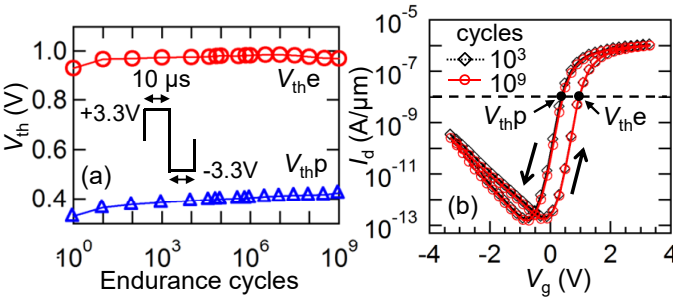

Fig. 3 3.3 V-operated V_{th} endurance (a) and I_d-V_g curves at 10^3 and 10^9 cycles (b).

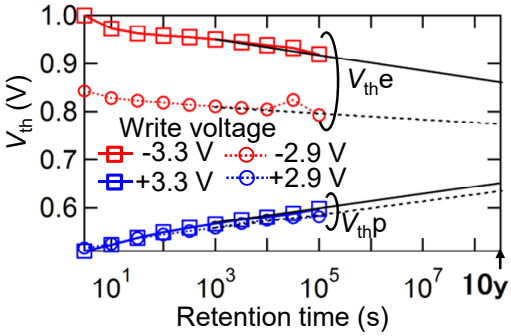

Fig. 4 3.3 V-operated V_{th} retentions.

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