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Technology challenges for future DRAM and NAND and technology breakthrough with emerging memories, MRAM and PRAM

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Abstract

There're much harsher process limits to advanced DRAM and NAND memories and also exactly different process limits to emerging memories these days. We researched the fundamental reasons for those limits for each device and suggested some innovative etching technologies to overcome them, new machines as well as new plasma chemistries, here.

1. Introduction

DRAM and NAND memories have been used widely for the various purposes so far, but as design rule decreases continuously for high density and cost down we confronted with the process limit to chip fabrication. The major process limit has been the etching of high aspect ratio(A/R) holes within storage cells, and so some alternative devices with lower stack height has researched. The promising candidates are MRAM and PRAM which were suggested to replace DRAM and NAND respectively. In addition IoT(Internet of Things), wearable devices and automotive electronics become major interest at the recent IT industry, and so the need of an embedded memory like STT-MRAM(Spin Torque Transfer MRAM) is soaring.[1]

Nevertheless these emerging memories also revealed critical process limits to mass production which occur at the MRAM MTJ(Magnetic Tunnel Junction) etching and the PRAM GST(Ge-Sb-Te) and OTS(Ovonics Threshold Switch) etching processes. The MTJ etching is very difficult since metals of the MTJ stack(Co, Fe, Mg, Pt, etc.) hardly form volatile etch byproducts, which byproducts are likely to redeposit on the sidewall of cells.[2,3] Ion milling as well as conventional RIE processes couldn't provide useful solutions for the MTJ etching [4,5] And the GST and OTS metal etching is also very harsh process because the excessive chemical reaction between halogen etchant radicals and metal atoms to generate easily the metal composition change of the GST and OTS.

We defined the process limits of DRAM and NAND memories and proposed some breakthrough technologies with conventional RIE(Reactive Ion Etch) system. And then we also modeled the process limits to the fabrication of the emerging memories, MRAM and PRAM, and we also suggested the breakthrough technology with an innovative IBE(Ion Beam Etch) system. These results will contribute the mass production of those memories in 2~3 year and the start-up of the much research on more innovative technology.

2. Fabrication of advanced memory devices

Capacitor hole etching is the most challenging technology at DRAM and its A/R has increased continuously so far. Fig.1 shows that the A/R kept nearly constant these days because innovative sensing technology was developed. But abrupt increase of the A/R is expected in the future and so the A/R amounts to 50% increase than the current level.

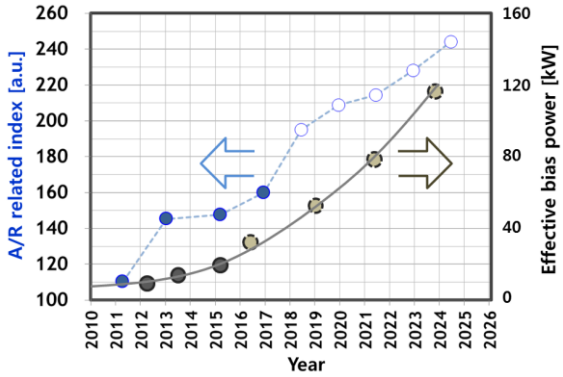
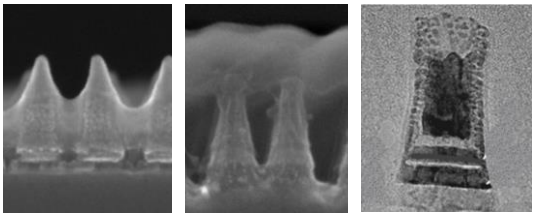


Fig. 1. A/R index and RF bias power trend of DRAM capacitor versus year.

For NAND memory its scheme had been kept the planar one until 2015 and it confronted the process limit to farther scale-down. But the innovative 3D NAND scheme emerged to provide the higher density cell chips without scale-down by stacking up many cell layers and this new scheme makes the D/R keep constant at the lower level than the conventional cells.

The severest process limit has been the etching loading which means the etch rate decreases with increasing the hole A/R. We have struggled to overcome this limit at DRAM and NAND fabrication and the most effective factor has been the higher bias power(BP) to provide higher energy ions. But this also induces another severe process limits, mask pattern collapse and tilted perpendicular profile.

We have researched the alternative memory devices without the high A/R structure and so MRAM and PRAM has suggested. For MRAM the most critical process is the etching of the nonvolatile MTJ metals and Fig. 2 shows the etch results with various methods. The etching with halogen gas chemistries gave much byproduct redeposit which occurs by very low volatility of the etch byproducts, and (C) shows better etch profile by sputtering by inert gases but the considerable metal redeposit remains at the cell sidewall.



(a) (b) (c)

Fig. 2. Images after MTJ etching with (a)Cl-based (b)F-based (c)Sputtering based tech.

We have studied the fundamental characteristics of atom sputtering process and we got to know that the ER's at sidewall and bottom side are dependent on ion energy and incident angle, ion mass. Fig. 3 shows much higher energy ion beam can give very vertical MTJ profile and no sidewall metal redeposit which generates MTJ cell current leakage, and so this technology is applicable for higher density memory cell.

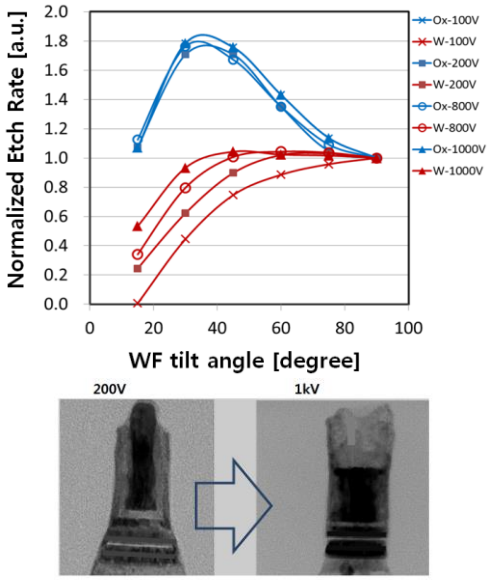


Fig. 3. Etch rate of Ar+ ion beam processes for different energy with varying WF tilt angles.

But this very high ion energy based etching makes unexpected surface damage which induces MTJ cell degradation as well as cell current leakage. Generally 20~30A deep surface damage remains just after high energy(~1,000eV) etching, which generates both MTJ degradation and MTJ leakage fail.

For PRAM the most critical issue has been the etch induced damage on GST and OTS metals and that damage comes mostly from easy reaction between halogen radicals and those metals atoms(Ge, Sb, As, Si and etc.).[6] We struggled to model the damage phenomenon and we knew that the control of the halogen radical amount is essential. Fig.4 shows the halogen chemistry makes severe damage of the atom composition shift of OTS metal compared with the Ar based chemistry. Fig. 5 shows that comparing with Ar only etching the low pressure gives the best result by low radicals and high outgassing from wafer surface. Generally the etch induced damage is more severe at GST etching due to its weak atomic bonding, and no radical etching technology may needed eventually.

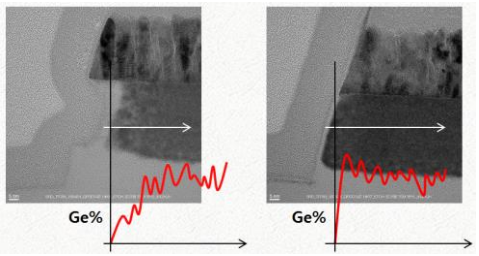


Fig. 4. Etch induced damage after the OTS metal etching. (left)HBr based etch and (Right)Ar based etch.

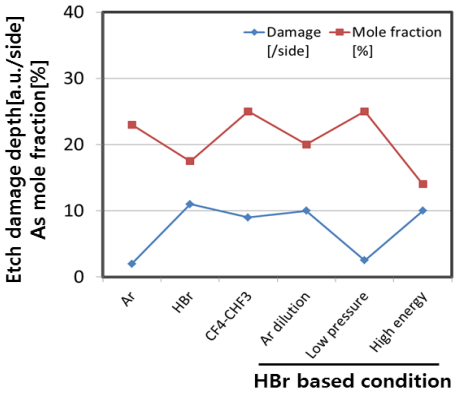


Fig. 5. OTS etch damage depth and As mole fraction after etching process according to many conditions.

3. Conclusions

We have researched to find innovative etching technologies for the advanced generation of DRAM, VNAND and the emerging memories of MRAM, PRAM, and we can suggest some valuable knowledge and technologies for each device. Consequently the controllability of radicals and ion energy for etching is key technology and we wish that these technologies contribute to more scalability and higher performance of those memory devices.

Acknowledgements

References

[1] Kangho Lee, Jimmy J. Kan, "United embedded non-volatile memory for emerging mobile markets", *ISLPED,* 131 (2014).

[2] R. E. Chapman, *J. Mater. Sci.* 12, 1125 (1977).

[3] R. E. Lee, *J. Vac. Sci. Technol*. 16, 164 (1979).

[4] H. Maehara, T. Osada, M. Doi, et al, Dig. *IEEE Intermag Conf.*, p. 1535. (2005)

[5] S. Takahashi, T. Kai, N. Shimomura, T. Ueda, et al, *IEEE Trans. agn*. 42, 2745 (2006).

[6] Sekoo Kang, Minhwan Jeon, "Etch damage of Ge2Sb2Te5 for different halogen gases", JJAP 50 (2011)