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N_2O-Treated Crystalline $ZrTiO_4$ as Charge Trapping Layer for Flash Memory Applications Featuring Low Operation Voltage

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I. Introduction

Conventionally, poly-Si that is electrically conductive has been adopted as the charge storage media for flash memory applications. However, the relatively thick tunnel SiO_2 (6~7 nm) and IPD (10~13 nm) not only limit vertical down scaling, but lead to high program/erase voltage in the range of 17~19 V. Due to these limitations, poly-Si has been replaced with Si_3N_4 which possesses discrete charge trapping sites. Unfortunately, Si_3N_4 is not a good charge storage media because of the shallow-level traps, small conduction band offset (ΔE_c) of 1.1 eV with SiO_2, large ΔE_c of 2.1 eV with Si substrate and relatively low dielectric constant (k) of 7. An ideal charge trapping layer (CTL) should have deep-level traps as well as a larger ΔE_c with tunnel dielectric for desirable charge storage and retention, a smaller ΔE_c with Si substrate for better charge injection, and a higher k value so that the electric field (E) over the SiO_2 tunnel dielectric can be higher due to electric flux density (D) continuity [1], making higher program/erase speed and lower operation voltage. Many high-k dielectrics such as HfO_2 [2], HfON [3], Al-doped ZrO_2 [4], La_2O_3 [5], and Y_2O_3 [6] have been extensively explored and exhibited promising memory characteristics. However, most high-k based CTLs are of amorphous phase with their k values rarely exceeding 25. Recently, phase transformation of a high-k dielectric from amorphous phase to crystalline one has attracted considerable interest since it provides an effective method to enhance the k value without compromising the band gap. The widely developed crystalline CTL mainly focuses on ZrO_2 [7, 8], with k value of 38.7 in tetragonal phase and 32.8 in cubic phase. Employing crystalline CTL indeed achieves lower voltage operation as compared to conventional amorphous CTL. To obtain a larger memory window (MW) at lower operation voltage, crystalline $ZrTiO_4$ in orthorhombic phase with k value of 46.8 [9] was explored as CTL in this work. Note that besides high k value, due to the incorporation of TiO_2 which is a small bandgap dielectric with a negative ΔE_c with Si substrate, $ZrTiO_4$ has a band structure more favorable than typical ZrO_2 or HfO_2 CTL in terms of a large ΔE_c with tunnel SiO_2 and a smaller ΔE_c with Si substrate, as shown in **Fig. 1**.

Orthorhombic $ZrTiO_4$ (o-ZTO) shows negligible memory characteristics. However, with additional N_2O plasma treatment on the o-ZTO, the memory performance significantly enhances was obtained in terms of a large memory window of 5.0 V by ±7 V bi-directional sweeping, a flatband voltage shift of 1.6 V by erasing at -7 V for 10 ms and desirable retention behavior, demonstrating the eligibility as a promising CTL for advanced flash memory.

II. Experiment

In the study, 3-nm SiO_2 thermally grown on p-type Si substrate was used as the tunnel oxide of the flash memory. Amorphous ZTO of 10.0 nm was deposited by PVD tool as the CTL. Then N_2O or CF_4 plasma treatment was performed on the CTL to investigate how incorporation of nitrogen or fluorine atoms affects memory characteristics. Next, 10-nm SiO_2 or Al_2O_3 respectively grown by CVD or ALD was deposited as the blocking oxide. TaN was subsequently deposited and patterned as the electrode. Finally, all samples were annealed at 700 °C to crystallize the CTL. Brief process flow are shown in **Fig. 2**.

III. Results and Discussion

(A). SiO_2 as Blocking Oxide

The x-ray diffraction (XRD) spectra shown in **Fig. 3** displays the impact of plasma treatment on the crystallization of ZTO after thermal annealing. It is observed that ZTO can be crystallized into o-phase without any plasma treatment. The crystallinity even improves with N_2O and CF_4 plasma treatment as evidenced by the sharper diffraction peak with higher intensity. **Fig. 4** shows the capacitance-voltage (C-V) hysteresis for N_2O-treated ZTO by bi-directional voltage sweeping and **Fig. 5** summarizes the dependence of sweeping voltage range on hysteresis MW. For ZTO without plasma treatment, it shows negligible MW and it can be inferred that a lot of oxygen vacancies arising from grain boundaries of o-ZTO contribute to shallow traps that can hardly store charges. For those with CF_4 plasma treatment, the MW is still too small to be detected. In fact, incorporation of F atoms into ZrO_2 CTL has been verified as a viable avenue to enhance memory performance [10]. The opposite phenomenon in this work can be understood by the x-ray photoelectron spectroscopy (XPS) F*1s* spectra shown in **Fig. 6**. Although abundant incorporation of F atoms into ZTO can be identified from the distinct binding energy peak of 684.38 eV. The peak greatly diminishes after thermal annealing. It is the absence of F atoms that makes CF_4-treated samples demonstrate negligible MW similar to those without any plasma treatment. On the other hand, N_2O-treated samples show noticeable MW which achieves 3.3 V by ±7 V sweeping. The reason why N_2O plasma induces desirable MW can be explained as follows. In the N_2O plasma, it will be decomposed into O and NO radicals. O radicals help passivate oxygen vacancies stemming from grain boundaries and therefore shallow-level traps can be mitigated. In addition, interface traps between CTL and tunnel SiO_2 can also be suppressed. Furthermore, NO radicals are responsible for generation of deep-level bulk charge traps which are favorable for charge storage without tunneling back to substrate or through blocking oxide. **Fig. 7** displays the C-V hysteresis measured at different frequencies. The frequency independent MW implies that charges are indeed stored in the deep-level CTL bulk traps rather than interface traps. **Fig. 8** shows the correlation between ln(J/E) vs. $E^{1/2}$ for N_2O-treated ZTO where J and E respectively denotes current density and electric field. The linear correlation suggests the current conduction through the ZTO is dominated by Poole-Frenkel mechanism and bulk traps are indeed generated during N_2O plasma treatment.

(B).Al_2O_3 as Blocking Oxide

Having confirmed N_2O-treared ZTO as a viable CTL, SiO_2 blocking oxide was replaced with Al_2O_3 and the C-V hysteresis curves for various sweeping voltages are shown in **Fig. 9**. **Fig. 10** displays that under ±7 V sweeping, the MW increases from 3.3 V to 5.0 V by changing the blocking oxide from SiO_2 to Al_2O_3, proving the effectiveness to enhance the E field over tunnel SiO_2. The desirable property is also manifested in the erase transient characteristics shown in **Fig. 11**. With -7 V erase voltage, the flatband voltage shift of 1.6 V can be obtained in 10 ms for Al_2O_3 blocking oxide, which is only 0.3 V for SiO_2 blocking oxide. **Fig. 12** reveals the retention performance measured at

room temperature (RT) and 85 °C. About 77.8 % charges are retained after 10^4 sec and 51.5 % charges are stored after 10-year operation by extrapolation.

IV. Conclusion

ZTO crystallized in orthorhombic phase was studied as the CTL in this work. Without any treatment, ZTO could hardly store charges due to a large amount of shallow-level traps induced by grain boundaries. By employing N_2O plasma treatment, undesirable shallow-level traps can be suppressed while generating deep-level ZTO bulk traps. With Al_2O_3 as blocking oxide, the memory devices can be operated at low voltage down to 7 V with satisfactory retention performance.

Acknowledgement

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References

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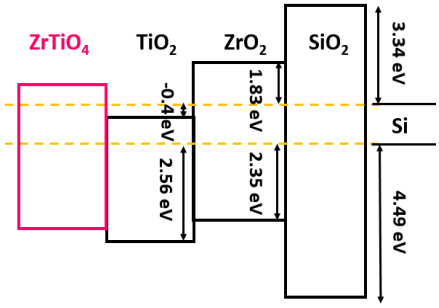

Fig.1 Band alignments for $ZrTiO_4$, TiO_2 and ZrO_2 with respect to SiO_2/Si system.

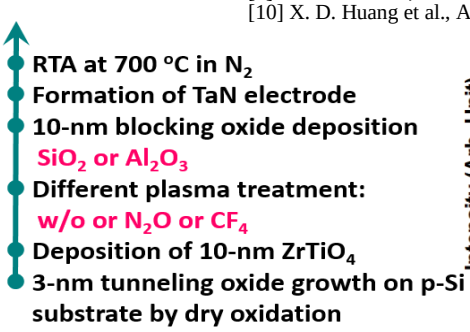

Fig. 2 Brief process flow for memory with $ZrTiO_4$-based CTL.

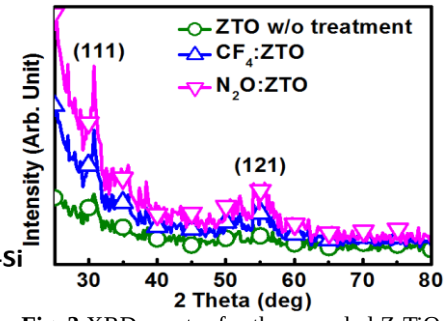

Fig. 3 XRD spectra for the annealed $ZrTiO_4$ films with different plasma treatment.

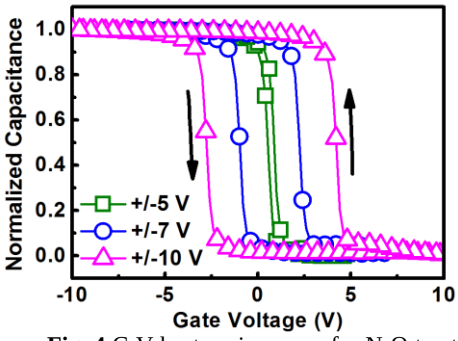

Fig. 4 C-V hysteresis curves for N_2O treated devices with SiO_2 as blocking oxide.

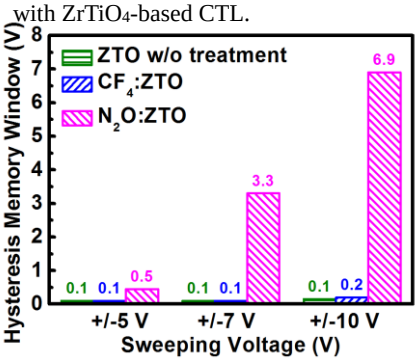

Fig. 5 Comparison of hysteresis MW for devices with various CTLs.

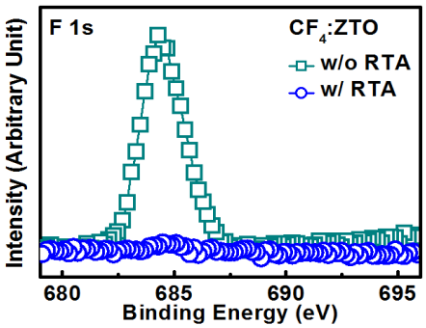

Fig. 6 XPS F 1s spectra for CF_4-treated $ZrTiO_4$ film with and without RTA.

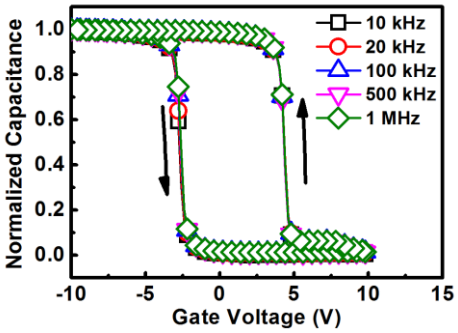

Fig. 7 Frequency dependent C-V curves N_2O treated devices with SiO_2 as blocking oxide.

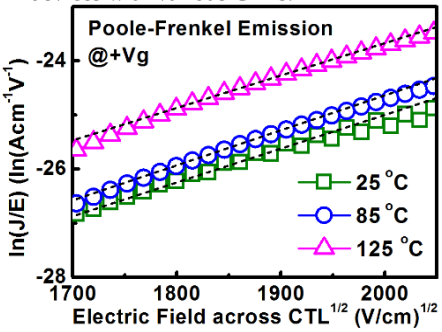

Fig. 8 P-F emission at 25 °C, 85 °C and 125 °C for devices with N_2O-treated CTL.

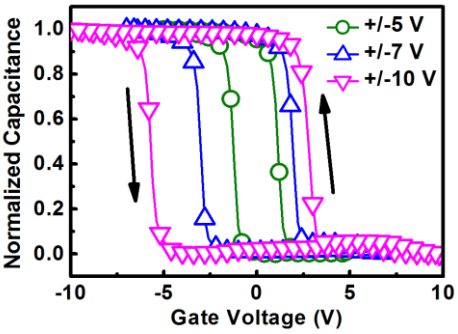

Fig. 9 C-V hysteresis curves for N_2O treated devices with Al_2O_3 as blocking oxide.

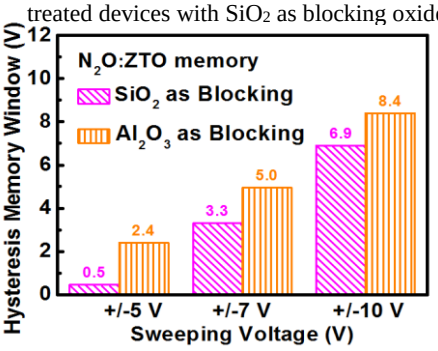

Fig. 10 Comparison of hysteresis MW for devices with different blocking oxides.

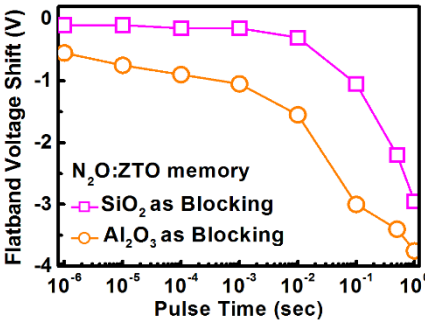

Fig. 11 Erase transient characteristics for devices with different blocking oxides.

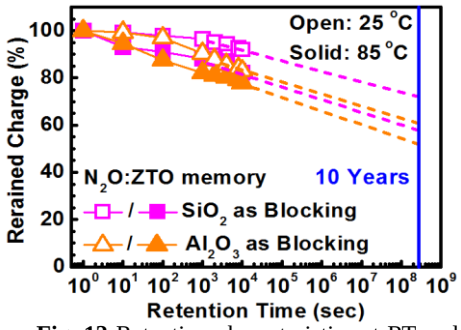

Fig. 12 Retention characteristics at RT and 85 °C for devices with different blocking oxides.