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Differential Multiple-Time-Programming Memory Cells by Laterally Coupled Floating Metal Gate FinFETs

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ABSTRACT

This letter presents a new differential multiple-time programmable (MTP) memory cell with a novel slot contact coupling structure in the FinFET CMOS process. This MTP cell contains a pair of floating metal gates to store differential data on a single cell. Through differential read operations, the cells are less susceptible to read err caused by cell-to-cell variations. In nano-scaled FinFET process, the gate dielectric layer becomes too thin to retain charge in floating gates for long period of time. Differential cell design further extends the data lifetime even with serious charge loss problem.

Introduction

With the growth of portable electronic products, logic non-volatile memory (NVM), fully compatible to CMOS logic process, is greatly in need for various IC modules requiring permanent data storage [1-2]. Key features of logic NVM technologies are low in cost, low voltage operations, flexible and adaptable to different generations of CMOS technologies. In advanced CMOS technology nodes, as gate dielectric thickness scaled to maintain good gate control, charge storage capability greatly reduced for floating gate based NVM cells [3-5]. Thus, it had become very hard to achieve the data retention lifetime exceeding ten years. In light of this challenge, logic NVM cells utilizing SiN trapping or resistive switching for data storage has been proposed in recent years [6-10]. However, floating gate (FG) devices are still the most favorable structure for cells which can sustain large numbers of write cycles. In this work, a differential FG multiple time programming memory cell has been proposed and demonstrated by 16nm CMOS FinFET technology. Differential FG cell increases the sensing window, and hereby enhance data lifetime. Benefitting from the high-aspect ratio metal gate in FinFET, novel laterally gate coupling structure through slot contacts can be realized with good area efficiency. To extend data lifetime of the FG devices, periodic refresh has also been investigated.

Cell Structure and Operation Principles

The proposed differential MTP samples investigated in the study are fabricated by 16nm FinFET CMOS logic process. A differential MTP cell consists of two identical floating gates and the corresponding select gates. The floating gate is composed of a transistor's metal gate connecting the read out channel and a coupling structure, as illustrated in Figure 1(a). As a result of high-aspect ratio metal gate in FinFET technologies, a large coupling capacitance between slot contacts and the floating metal gate is readily available. By placing of long slot contacts closely to the FG over STI regions, an effective coupling structure can be obtained. The cross-sectional TEM in the coupling region is shown in Figure 1(b), indicating that the slot contacts can be placed with a narrow spacing to the MG of less than 200nm.The coupling ratio is directly proportional to the length of the contact slots, which is connected to the control line (CL).With a contact length of 1.5μm, the coupling ratio of the cell can reach 0.4. The transistor section allows for channel hot electron (CHE) injection for programming and drain-side Fowler-Nordheim (FN) tunneling for erasing, as illustrated in Figure 1(c). Furthermore, the differential MTP cells can be arranged in a NOR-type array, as shown in Figure 2. In the memory array, drain of the transistors are connected to the bit line(BL), while source and gate of the select transistor are connected to the source line (SL) and the word line (WL), respectively. The slot contacts in the coupling structure is connected to a common control line (CL). The cell layout and the array circuit schematic are shown in Figure 2 and Figure 3, respectively. Threshold voltage shift revealed by the IV characteristics in Figure 4 can be obtained by CHE program and FN erase, successfully. For programming, the optimized operating point can be found by monitoring the gate current of a dummy device, as shown in Figure 5. The measured gate current vs. V_{CL} corresponds to the injection current to the FG during programming. As expected, maximum injection current occurs at V_{BL}~V_{FG}. For a coupling ratio of 0.4, optimal bias voltage for CHE program is around 7V. Time-to-program and time-to-erase characteristics of this cell are compared in Figure 6. To avoid junction breakdown, V_{BL} is set to 3V. The maximum programming speed is found at V_{CL}= 7.5V, agreeing with the data in Figure 5. For erase operations, V_{CL} is set to -6V for an erase time of less than 100ms. For read operations, V_{CL}, V_{WL} and V_{BL} are all set to 0.8V (V_{DD} for core devices) for reaching a read current of 10μA. The operation conditions for this MTP cell are listed in Table 1.

Reliability Evaluations

For endurance tests, the threshold voltage of program and erase states are monitored during P/E cycling. The test results are shown in Figure7 reveals that the sensing window remains stable after 100k P/E cycles. Program disturbance characteristics on cells sharing a common BL is shown in Figure 8. Data suggest that an unselected cells can subject 10^4 program cycles with significant shift in V_{th} at both states. The differential data is stored in the two FGs in a cell, i.e., FG1 is in the program state and FG2 is in the erase state or vice versa, to increase sensing window. For data retention tests at elevated temperatures are performed. Due to the thin gate dielectric of less than 4nm, the threshold voltage window narrows fairly quickly with time, as expected, see data in Figure 9. A failure criteria of threshold voltage difference of less than 0.6V is set for finding the Time to failure (TTF) for this cell. At 85ºC, the data lifetime is 10^6 seconds, while at 150ºC, it reduces to $1.4x10^5$ seconds. The data lifetime of this differential cell at room temperature can be obtained by extrapolation, as shown in Figure10, projects a time-to-failure of 189 days at room temperature. This means that the data in this MTP need to be periodically refresh to avoid data lost. For commercial ICs, 85ºC is generally the specification limit. Thus, periodic refresh test are performed for cells bake at 85ºC. As shown in Figure 11, the cell need to be refreshed once every 3 days to ensure enough V_{th} different between the two devices. Even with gate dielectric thickness of less than 4nm, this differential FinFET MTP cell can still maintain its data effectively with periodic refresh cycles.

Conclusions

A differential FinFET MTP cell which is fully compatible to FinFET logic process is proposed and demonstrated, here. To overcome the charge lost problem of floating gate devices in advance CMOS technologies, this MTP cell adapts both a differential structure and a periodic refresh scheme. In addition, the new MTP cell features effective laterally coupling structure, increases sensing window and simplicity in its periphery circuits, most suitable for logic NVM applications.

Acknowledgement

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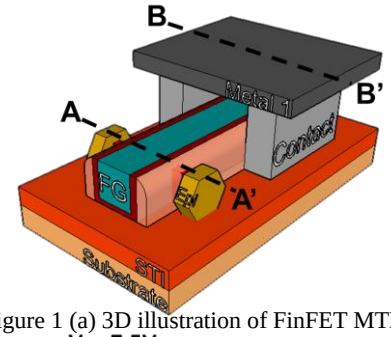

Figure 1 (a) 3D illustration of FinFET MTP.

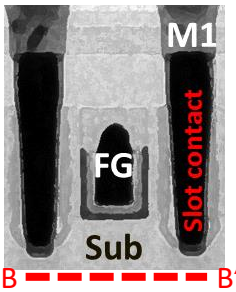

Figure 1 (b) TEM of the FinFET MTP's coupling structure.

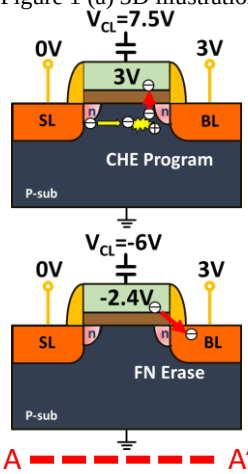

Figure 1 (c) Coupling ratio of the MTP cell is 0.4. Channel hot electron (CHE) injection is used to program the FG1, while Fowler-Nordheim (FN) tunneling is used to pull electrons out of the complementary FG2.

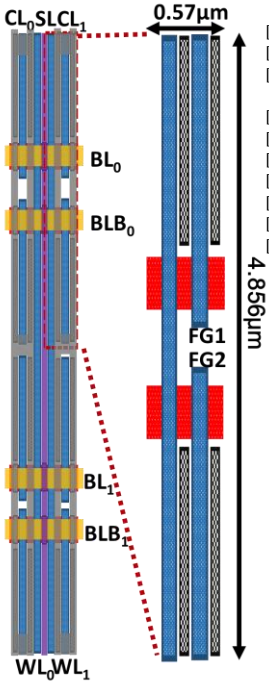

Figure 2 The 2x2 NOR-type array layout and an unit cell size of 2.768μm^2 can be achieved.

References

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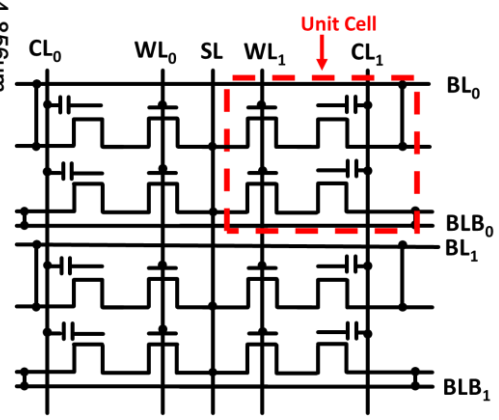

Figure 3 An illustration of 2x2 NOR-type array, where differential BLs crossing parallel WL and SL to ensure proper selections.

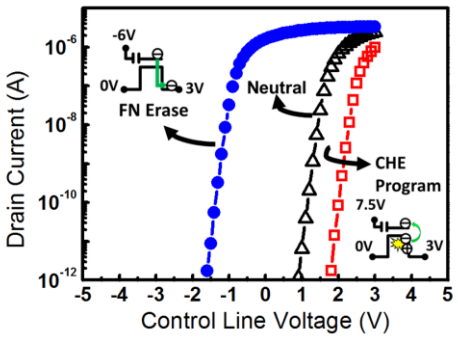

Figure 4 Differential MTP can be successfully program and erase by CHE and drain-side FN with an enlarged sensing window.

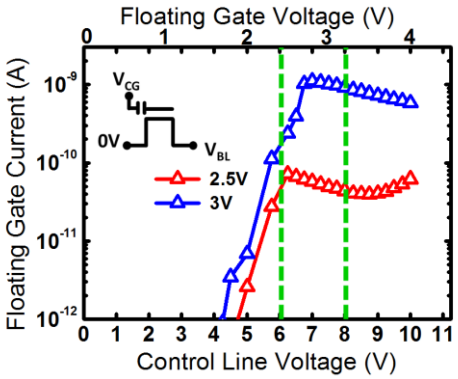

Figure5 Maximum programming efficiency occurs at drain voltage is equal to floating gate voltage, corresponds to V_{CL}~6-8V.

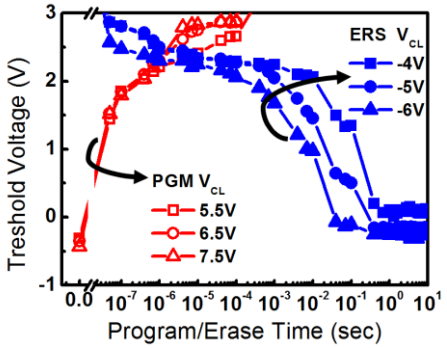

Figure 6 Time to program and time to erase characteristics at V_{SL}=0V, and V_{BL}=3V at different CL voltages.

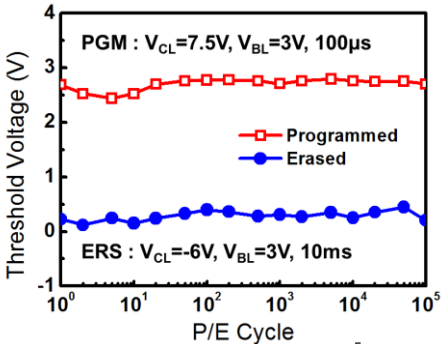

Figure 7 P/E characteristics up to 10^5 cycles, showing stable V_{th} for cells at both states.

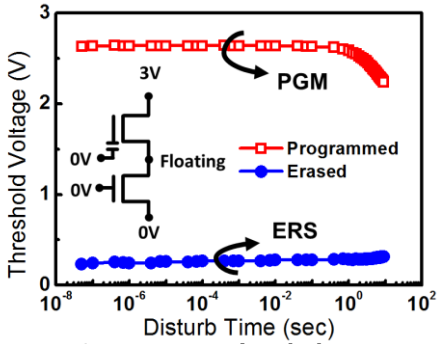

Figure 8 Programming disturb characteristics for cells sharing the same BLs.

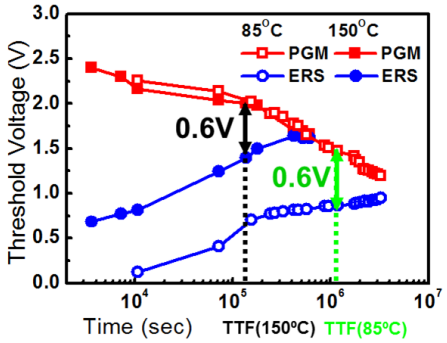

Figure 9 Data retention characteristics of cells under 85°C and 150°C, respectively.

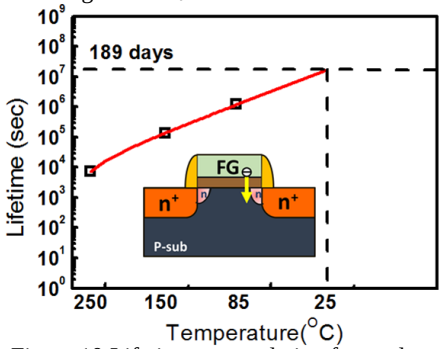

Figure 10 Lifetime extrapolation for read margin no less than 0.6V. At room temperature, The TTF of a differential MTP cell is closed to 6 months.

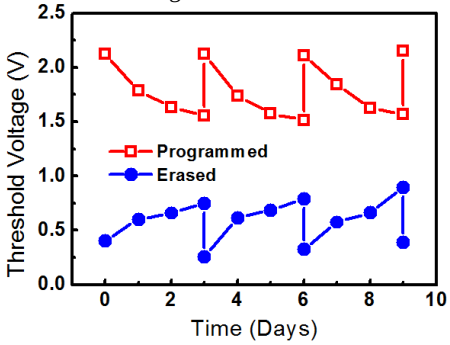

Figure 11 Based on general commercial IC's specification of 85° C, stored data need to be refreshed every 3 days.

	WL	BL BLB	CL
PGM	1.8V	3V	7.5V
ERS	0V	3V	-6V
Read	0.8V	0.8V	0.8V

Table 1 Operation conditions of the differential FG MTP memory in 16nm FinFET technologies. V_{SL} remains 0V at all times. Whereas unselected cells are inhibited by setting V_{BL}=V_{BLB}=0 and V_{WL}=0.