Analog VLSI Circuits and Devices for Neuro-Inspired Time-Domain Computing

Takashi Morie

Kyushu Institute of Technology

2-4, Hibikino, Wakamatsu-ku, Kitakyushu, Fukuoka 808-0196, Japan Phone: +81-93-695-6122 E-mail: morie@brain.kyutech.ac.jp

Abstract

Although different neuron models have been proposed so far, basic neuron models are commonly expressed by differential equations about the internal potential of a neuron. Since using capacitors to store internal potentials is a natural circuit implementation of these models, analog VLSI implementation is suitable for them. As neuro-inspired time-domain computing, we have implemented various types of processing models in which spike-based computations are performed during a capacitor charging operation. We review in this paper these models and their analog VLSI implementations. Requirements for novel devices to apply such implementations are also addressed.

1. Introduction

In spiking neural network models, neurons interact with each other via synapses with asynchronous spike pulses [1]. Each neuron has its analog internal potential, which is updated by the responses generated by input spikes. As VLSI implementation of these models, it is natural to use a capacitor to store the internal potential and to update it by current sources connected with the capacitor. Output spike pulses are created by thresholding the internal potential with a comparator. Connections between neurons are expressed by synaptic weights, and analog memory devices are being developed for storing and modifying the weights by learning algorithms in artificial neural network models.

In this paper some neuro-inspired time-domain computing models and their VLSI implementations are reviewed.

2. Circuits and devices for time-domain computing

The basic circuit configuration for time-domain computing is shown in Fig. 1. In digital VLSI implementation, an up/down counter is usually used to store and update the internal potential of a neuron [2], in which digital circuits have to operate at each update timing synchronizing with a clock signal. This operation is inefficient and increases power consumption.

On the other hand, in the analog VLSI implementation, we use a capacitor charged with current sources switched by spike pulses. To guarantee the calculation precision or resolution in the time domain, the operation time range should be set on the order of 1 μ s. Although this speed is 1,000 times slower than that of the current digital circuits, massively parallel processing in analog VLSI implementation can overcome this slow speed. Furthermore, parallel processing during a single charging operation to a capacitor can

lead to higher performance and dramatically lower power operation compared to state-of-the-art digital VLSI implementation. For example, if we use a 10-fF capacitor with a 0.1-nA current source at 1-V supply voltage, an energy consumption of 10 fJ is achieved.

Although the gate capacitance of a current FinFET is less than 1fF [3], parasitic capacitance related to interconnection is comparable to this value. Therefore, reduction of such parasitic capacitance is a challenge to achieve extremely low power consumption operation. It is also a challenge to flow a sub-nA order current with low device variation or to fabricate a high resistance on the order of more than 1 G Ω . We have succeeded in fabricating nanodisk array structures that can realize resistance of more than 1 G Ω , using new fabrication technology that combines bio-nanotemplates and neutral beam etching [3].

It is also a big challenge to develop nonvolatile analog memory devices not only for realizing learning mechanisms that mean updating the connections between neurons but also for compensating timing variations due to device mismatches and/or timing delay due to parasitic capacitance.

3. Neuro-inspired time-domain processing models and their VLSI implementations

We have been developing neuro-inspired circuits and analog VLSI chips based on time-domain computing. Some examples are briefly reviewed as follows.

Integrate-and-fire neuron for weighted-sum calculation

Weighted-sum calculation is an essential function for intelligent processing. A method to perform this calculation based on a spiking neuron model was proposed [4], and we have proposed and demonstrated its implementation based on time-domain computing using a nanodevice [3]. Linear response rising at input spike timing is assumed and time-domain summation is achieved, as shown in Fig. 2.

Pulse-coupled oscillator systems for coupled Markov random field (MRF) models

In a period of oscillation in the internal potential ϕ from 0 to 2π , a small modification is performed by the value of the coupling function Z at the timing of a spike *spk* from another neuron, as shown in Fig. 3. Since at this timing, the internal potential value of the neuron sending a spike is zero, the value of the coupling function of the difference between the internal potential values of the interacted neurons is added to the internal potential. Using this property, we have successfully implemented the coupled MRF model in the time domain [5].

Oscillator-based chaotic Boltzmann machines

The chaotic Boltzmann machines (CBMs) are a model operating chaotically and can be replaced with the original Boltzmann machines (BMs) that operate stochastically [6]. In the VLSI implementation of BMs, we have to incorporate random number generators for original BMs, but CBMs can be implemented in analog VLSI circuits based on an oscillator model operating deterministically. In the dynamics of CBMs, the internal potential change is modified when the weighted sum of other neurons' states changes, as shown in Fig. 4.

4. Conclusions

Neuro-inspired time-domain computing is basically suitable for extremely low power operation because multiple calculations can be achieved in a single charging operation to a capacitor. The challenges are the development of circuit elements with high precision such as current sources with a current of sub-nA or high resistance with more than 1 G Ω . Novel analog memory devices are also desired to compensate for variation of the circuit elements as well as to implement learning function.

Acknowledgements

This work was supported by JSPS KAKENHI Grant Nos. 22240022 and 15H01706. Part of the work was carried out under the Collaborative Research Project of the Institute of Fluid Science, Tohoku University.

References

- W. Maass and C. M. Bishop, Eds., *Pulsed Neural Networks*, MIT Press, 1999.
- [2] Y. Suedomi et al., Neurocomp. 165 (2015) 54.
- [3] T. Tohara et al., Appl. Phys. Express 9 (2016) 034201.
- [4] W. Maass, Neural Computation 9 (1997) 279.
- [5] K. Matsuzaka et al. Electron. Lett. 51 (2015) 46.
- [6] H. Suzuki et al. Sci. Rep. 3 (2013) 1610.



Fig. 1 Circuit configuration for time-domain computing: (a) digital approach and (b) analog approach.



Fig. 2 Integrate-and-fire neuron for weighted-sum calculation: (a) timing diagram, (b) circuit configuration, and (c) algorithm.



Fig. 3 Pulse-coupled oscillator systems for coupled MRF models: (a) positive update, (b) negative update, (c) oscillator circuit, and (d) dynamics of a coupled MRF model, which has two variables fand θ as ϕ , and four coupling functions A, B, C, and S as Z.



Fig. 4 Oscillator-based chaotic Boltzmann machines: (a) timing diagram, (b) circuit configuration, and (c) dynamics.