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HIGH EFFICIENCY AND LOW POWER HORIZONTAL CAPACITIVE MODULATORS FOR 56Gb/s

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Abstract

We present TCAD simulation results for capacitive modulator integration in a 300mm SOI photonics platform. We find a trade-off between bandwidth and component efficiency with 13nm thick capacitor oxide. The design, as compact as 820µm active length for 4.5dB extinction ratio, operates at 56Gb/s with low power consumption (0.37pJ/bit at 0.9Vpp swing).

1. Introduction

Optical carrier modulation is a key challenge in silicon photonics transmission lines[1,2,3]. Using a Mach Zehnder interferometer as amplitude modulator, we design a capacitive phase shifter (CPS) embedded on each optical path of the interferometer. To be competitive, this photonic device must achieve a good trade-off between high bandwidth, low power consumption, large phase shift and low insertion losses (IL). While mature technologies provide 25Gb/s bandwidths with PN junction phase shifters[4], CPS development has already demonstrated 8dB extinction ratio at 40Gb/s with only 6.5dB/mm IL[5,6]. CPS operate at narrow voltage swings with respect to PN junctions, thus leading to low power consumption for both the electro-optic phase shifter and the electronic integrated circuit. We propose a new CPS device targeting low power consumption and 56Gb/s data rates, compatible with 300mm silicon photonics platform[4]. We describe the simulated device in section II, section III is devoted to device performances and trade-offs to reach low power consumption and high data-rates.

2. Simulated Device Description

Process Flow

CPS consists of two arms overlapping on an interfacial oxide to build up a capacitor in the device optical path. The right arm (Fig. 1a) of the capacitor is made up of patterned 300nm thick Silicon-On-Insulator (SOI). The SOI is encapsulated with oxide and implanted with Boron. The left arm, made up of deposited amorphous Silicon, is defined by opening a cavity in the planarized oxide above the patterned SOI. Using damascene-like front-end process steps[7], one can expect low interface defect density and low charged defects in the oxide. After planarization, the left arm top is aligned with the SOI top, allowing the use of a standard back-end process flow. After crystallization and poly-Si patterning, the capacitor active region serves as optical waveguide (WG) in the structure center (Fig. 1b).

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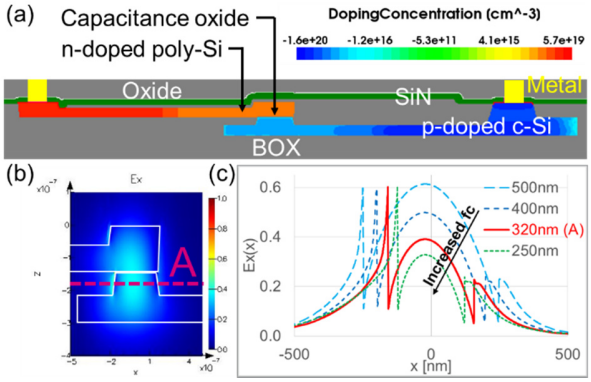

Fig. 1 (a) Process Simulation of the active dopants (2D cut), (b) Fundamental TE mode, (c) $E_x(x)$ cut for different WG widths.

Electro-Optic Simulation

Free carrier densities and electrical admittance are simulated with Sentaurus Process and Device software[8]. A voltage difference between the anode and the cathode (respectively left and right metal contacts in Fig. 1a) is swept from -0.5V to 1.8V. We extract free carrier densities for each value of the potential difference and 1.8V admittance $Y(\omega) = G(\omega) + j\omega C(\omega)$). We then calculate the transfer function

$$H = \sqrt{1 + \left(\frac{G(\omega)}{\omega C(\omega)}\right)^2}^{-1}$$

giving the -3dB cut-off, corresponding to the series $R_S C_S$ filter bandwidth with $C_S = C(LF)$. Electro-optic conversion is achieved[9] by using Soref coefficients[10] to interpolate the 2D n,κ(x,y,V) matrix. Regular output mesh step is around 5Å. Lumerical MODE software[11] finally calculates the resulting guided fundamental TE mode effective index in the active capacitor WG. From the effective index variation with the potential Δn_{eff}, the phase shift is $\Delta\varphi = \frac{2\pi}{1.31\times10^{-3}}\Delta n_{eff}$. The imaginary part at 1.8V indicates worst case IL. Phase shift error convergence is to the nearest 2.5°/mm, the absorption to 10^{-4}dB/mm.

3. Capacitive Modulator Design

WG Optimal Design

The capacitor device consists of a TE rib WG with two slabs for the electric contact and optimized for polarization stability and mode confinement/bandwidth trade-off. Shallow slab patterning (100nm thick) provides low access resistances for bandwidth optimization. Mode peak intensity position with respect to the active region is driven by the slab thickness ratio.

The bottom slab can be as thin as 80nm to shift the mode peak upward with 10% decrease of both the bandwidth and the total losses (including 7% active length decrease).

The WG width w_{WG} [nm] also contributes to the bandwidth/confinement trade-off. The cut-off frequency increases with decreasing w_{WG}, following:

$$f_c = \frac{1}{2\pi R}\frac{1}{C_{ox}} = \frac{1}{2\pi R}\frac{t_{ox}}{\varepsilon_{ox} w_{WG}} \quad (1)$$

Where C_{ox}[F/mm] is the oxide capacitance, R[Ω.mm] the series resistance, t_{ox} [nm] the capacitor oxide thickness, and ε_{ox}[F/mm] the oxide permittivity ($\varepsilon_r = 3.9$). Without shallow slab patterning, the mode area is hardly decreased with w_{WG}, a good overlap factor is provided by a wide capacitance only, limiting the device speed. With a shallow etch, the width can be shrunk down to 300nm width (Fig. 1c).

Bias Point Optimization

To derive the best bias point of our device with the lowest dynamic power, we vary the applied voltage between the electrodes. We plot the phase shift with respect to 0V effective index, and IL per unit length (Fig. 2).

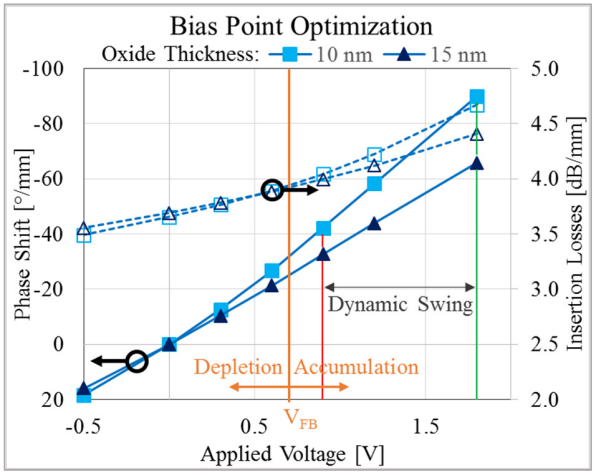

Fig. 2 Phase Shift and IL (low material absorption: κ_{Si}=3.8x10^{-6}) for N_{dop}=1.1x10^{18}cm^{-3}

The free carrier swing is obtained by charging the capacitor ($Q = C_{ox}V$) with majority carrier accumulation. While the depletion regime is $\sqrt{V}$-dependent below the Flat-Band voltage V<V_{FB}=0.7V, the phase shift is almost linear in accumulation (Fig. 2). The voltage swing can be decreased to 0.9Vpp to gain in dynamic power consumption ($E_{bit} = C_{ox}(t_{ox}, L)V_{pp}^2/2$). Applying a DC bias of 1.35V, we shift the voltage swing in the linear regime where a higher modulation efficiency compensates the voltage swing decrease.

The highest loss level arises at 1.8V, consisting of: mode intrinsic losses (0.16dB/mm), poly-Si estimated losses (1dB/mm[12]), doping level losses (~3.7dB/mm at 1.1x10^{18}cm^{-3}), and losses from free carrier accumulation at oxide interfaces (<1dB/mm).

For $t_{ox} = 13.4nm$, the simulated oxide capacitance is ~1.1pF/mm. In the next section, we look for the shortest devices to reach <1pJ/bit power consumption at 0.9Vpp swing and 30° phase shift (4.5dB extinction ratio).

Performance Trade-offs

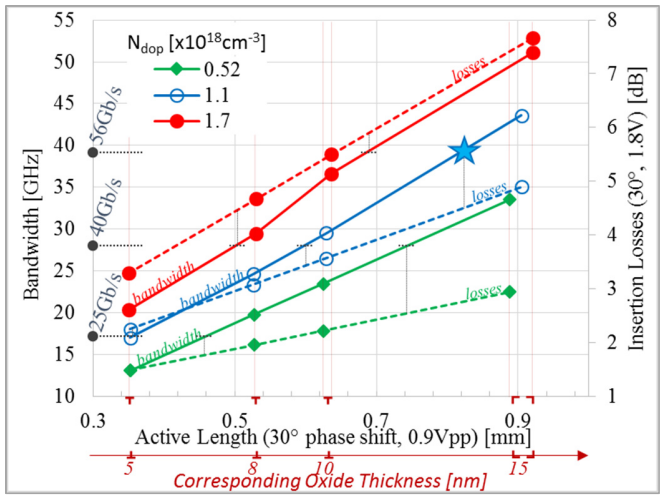

Fig. 3 Bandwidth / IL Trade-off

CPS device efficiency increases with decreasing oxide thickness at the cost of the bandwidth (Fig. 2 and Fig. 3), due to a capacitance increase (Eq. 1). We target ~800µm active region length for a 30° phase shift. IL are increased with the doping level and less significantly with the length. We target 4dB total losses (including 1dB/mm[12] poly-Si absorption). Since the energy per bit (< 0.4pJ/bit) is marginally decreased with the doping level, we must optimize IL with the lowest doping level. We summarize the performances of the device in the following table for each data-rate target:

	Ref [5]	[6]	This work**		
Datarate [Gb/s]	40	2.4	25	40	56
Voltage Swing [V]	1	1.5	0.9	0.9	0.9
Oxide Thickness [nm]	-	5	7	12	13.4
Doping Level [x10^{18} cm^{-3}]	-	1	0.52	0.52	1.1
30° Shift Length [µm]	330	530	470	740	820
Total Losses (30°) [dB]	2.145	3	1.3	1.8	4.5
E_{bit} [pJ/bit]	< 3 (*)	0.18	0.34	0.36	0.37

*complete path **simulations

4. Conclusion

We present the design of a horizontal oxide CPS, optimized for 40Gb/s and 56Gb/s data-rates. Low power consumption (0.37pJ/bit) is the main advantage of CPS thanks to their low AC operating amplitude (0.9Vpp), interesting for the external driver consumption as well.

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