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Waveguide-Integrated Vertical pin Photodiodes of Ge Fabricated on p^+ and n^+ Si-on-Insulator Layers

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Abstract

Waveguide-integrated vertical pin photodiodes (PDs) of Ge epitaxial layers are fabricated on Si-on-insulator (SOI) layers with two different conduction types of p^+ and n^+, and the performances are compared between n^+-i-p^+ on p^+-SOI and p^+-i-n^+ on n^+-SOI. Both types of PDs show good responsivities more than 0.5 A/W at 1.55 μm, while the dark leakage current is larger for p^+-i-n^+ PDs on n^+-SOI. Possible mechanism is discussed to explain the observed difference in the leakage current.

1. Introduction

Ge efficiently absorbs near-infrared (NIR) light used in the optical communications (1.3 – 1.6 μm). Due to the compatibility of Ge with Si CMOS processes, Ge has been applied to NIR photodiodes (PDs) in Si photonics. The authors have been reported high-performance pin PDs of Ge epitaxial layers integrated with Si-on-insulator (SOI) waveguides [1 – 3]. The fabricated PDs possess a vertical n^+-i-p^+ structure on p^+-SOI layer. This n^+-i-p^+ configuration was suggested to show better performances in terms of dark leakage current [4]. However, the inverted configuration of p^+-i-n^+ on n^+-SOI is sometimes effective to send an electrical signal from the p^+ contact to a transimpedance amplifier.

In this work, waveguide-integrated vertical pin PDs of Ge epitaxial layers are fabricated on SOI layers with two different conduction types of p^+ and n^+, and the performances are compared between n^+-i-p^+ on p^+-SOI and p^+-i-n^+ on n^+-SOI.

2. Fabrication

Ge PDs integrated with Si waveguides, shown in Fig. 1, were fabricated. An SOI wafer with 200-nm-thick top (001) Si layer was used as the starting substrate. First, Si optical waveguides with the width of 440 nm were fabricated. At the edge of each Si waveguide, p^+ or n^+ Si slab regions were prepared with boron or phosphorous ion implantations, on which n^+-i-p^+ or p^+-i-n^+ PDs of Ge were formed. On the slab region, a mesa-shaped Ge epitaxial layer (600 nm in thickness) was selectively grown by ultrahigh-vacuum chemical vapor deposition with SiO_2 masks. On the top of mesa structure, n^+ or p^+ region was formed by the ion implantation. The size of n^+ or p^+ region on the top, referred to as the PD size, was typically 5 μm × 30 μm. Finally, metal electrodes were formed. Current-voltage (I-V) characteristics at room temperature were measured with and without the illumination of 1.55-μm light propagated through the Si waveguides. Responsivity was estimated, taking into account the propagation loss in the waveguide (~ 3 dB/cm) as well as the coupling loss between the input optical fiber and the Si waveguide. I-V characteristics at different temperatures (0 – 100˚C) were also measured under dark in order to discuss the difference in the dark leakage current between the n^+-i-p^+ PDs on p^+-SOI and the p^+-i-n^+ PDs on n^+-SOI.

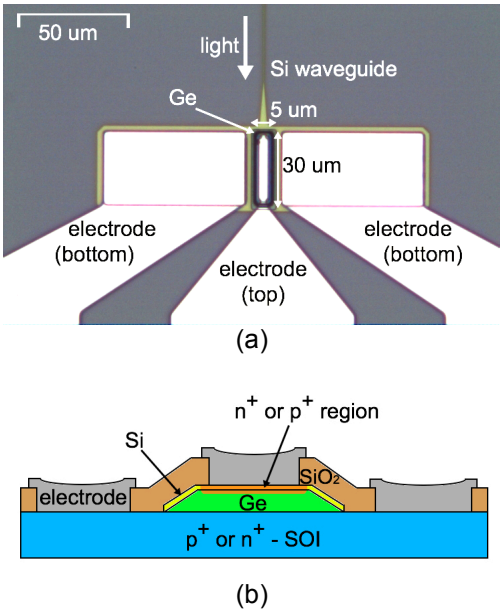

Fig. 1 (a) Typical optical microscope image and (b) schematic cross-section for Ge PD integrated with Si waveguide.

3. Results and Discussions

Figures 2(a) and 2(b) show I-V characteristics with and without the illumination of 1.55-μm light propagated through the Si waveguides for n^+-i-p^+ PDs on p^+-SOI and p^+-i-n^+ PDs on n^+-SOI, respectively. The size of PDs was 5 μm × 30 μm. Both types of PDs showed good rectifying diode properties, and photocurrent was successfully detected. The responsivity was estimated to be, at least, 0.5 A/W, taking into account the coupling and propagation losses, showing high photodetection efficiencies.

However, the dark leakage current under the reverse bias was larger for p^+-i-n^+ PDs on n^+-SOI than that for n^+-i-p^+ PDs on p^+-SOI, being similar to the previous report for PDs fabricated on bulk Si wafers [4]. The dark current for n^+-i-p^+ PDs on p^+-SOI showed a low value of 0.02 μA at the 1-V reverse bias, corresponding to the current density as small as 10 mA/cm^2, while the current for p^+-i-n^+ PDs on n^+-SOI

showed an increased value of 2 μA at 1 V, corresponding to the density as large as 1000 mA/cm^2.

Figure 3 shows I-V characteristics under dark measured at different temperatures. For both types of PDs, the dark current increased with the temperature. Arrhenius plots in Fig. 4 showed linear dependences for both types of PDs, although the activation energies were different. The activation energy for n$^+$-i-p$^+$ PDs on p$^+$-SOI was 0.33 eV for the temperature higher than room temperature. This value is almost equal to the half of bandgap energy for Ge, indicating that the dark current is ascribed to the thermal generation of carriers via mid-gap defect levels in Ge [1]. On the other hand, the activation energy for p$^+$-i-n$^+$ PDs on n$^+$-SOI was nominally 0.25 eV, which is smaller than that for n$^+$-i-p$^+$ PDs on p$^+$-SOI. This suggests that the mechanism to cause the dark current is ascribed not only to the thermal generation of carriers but also to other mechanisms such as surface leakage as well as formation of leakage paths induced by dopant diffusion and/or ion implantation for the top contact, although further studies are necessary to clarify this point.

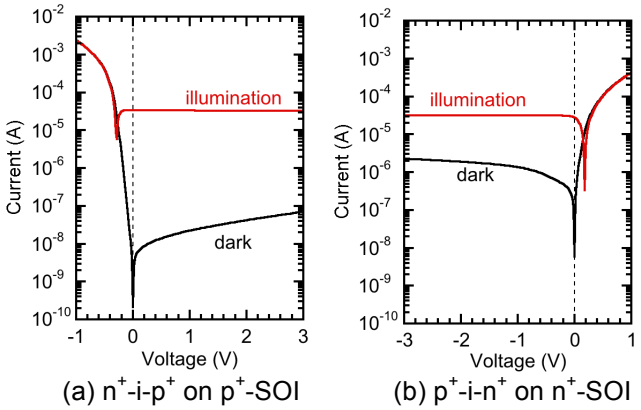

Fig. 2 Typical I-V characteristics with and without the illumination of 1.55-μm light. (a) for n$^+$-i-p$^+$ PDs on p$^+$-SOI and (b) for p$^+$-i-n$^+$ PDs on n$^+$-SOI.

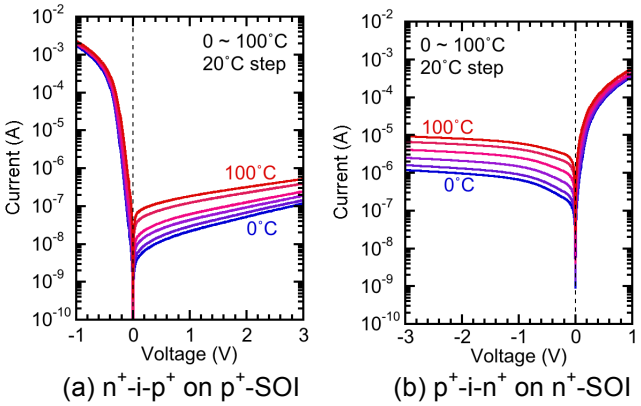

Fig. 3 Typical I-V characteristics under dark measured at different temperatures. (a) for n$^+$-i-p$^+$ PDs on p$^+$-SOI and (b) for p$^+$-i-n$^+$ PDs on n$^+$-SOI.

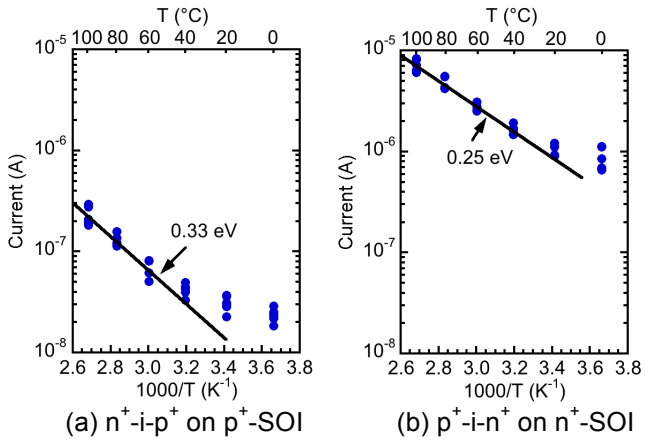

Fig. 4 Arrhenius plots of dark leakage current at 1 V reverse bias. (a) for n$^+$-i-p$^+$ PDs on p$^+$-SOI and (b) for p$^+$-i-n$^+$ PDs on n$^+$-SOI.

4. Conclusions

Waveguide-integrated vertical pin PDs of Ge epitaxial layers were fabricated on SOI layers with two different conduction types of p$^+$ and n$^+$, and the performances were compared between n$^+$-i-p$^+$ on p$^+$-SOI and p$^+$-i-n$^+$ on n$^+$-SOI. Both types of PDs showed good responsivities more than 0.5 A/W at 1.55 μm, while the dark leakage current was larger for p$^+$-i-n$^+$ PDs on n$^+$-SOI. The temperature dependence of dark leakage current suggested that the dark current for p$^+$-i-n$^+$ PDs on n$^+$-SOI is ascribed not only to the thermal generation of carriers but also to other mechanisms.

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