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Suspended Ge Gate-All-Around Nanowire FETs with Selective Etching Technique

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Abstract

This study presents a simple and cost-effective method to fabricate nearly defect-free Ge nanowires (NWs) for gate-all-around (GAA) FETs integration. A sequential selective etching process to remove residual Si and Ge near defective Ge/Si interface of epitaxial Ge grown on SOI is investigated. The orientation and temperature dependence of Ge/Si for selective etching indicates the selectivity between Ge and Si on different direction or orientation is controllable. We also demonstrate a suspended Ge GAA nanowire nFET (nNWFET) with CMOS compatible technology.

Introduction

The enhanced performance and cost reduction of Si electronic devices depends on steady downscaling of CMOS dimension in VLSI industry over past two decades. Fundamental factors such as short channel effects (SCE) and rising gate leakage current ultimately limit CMOS scaling. Integration of high-mobility channel materials on Si substrates is essential beyond sub-7 nm node in VLSI technology [1]. Ge has emerged as a promising alternative channel material for high performance CMOS. However, the higher permittivity degrades the electrostatic integrity and the narrower bandgap results higher band-to-band-tunneling (BTBT) leakage. For reducing leakage current and standby power consumption, GAA structure [2-3] is adopted to suppress short channel effects in Ge devices. Epitaxial Ge grown on SOI substrate prevent substrate leakage current with buried oxide (BOX) blocking the path. The other sneaking path beneath S/D still exists where there are plenty of stacking faults near Ge/Si interface. The dislocated Ge/Si region contributes high leakage current. This work takes advantage of chemical selective etch to realize suspended Ge nanowires which completely remove Si seed layer and partially dislocated Ge region near Ge/Si interface. The selective etching process eliminates the stacking faults which are produced intrinsically during Ge epitaxy process on SOI substrate. This key selective etching process is followed by H_2O_2 solution chemical etching which is further downscaling the dimension of Ge nanowires and realize Ge nNWFETs with superior electrostatic integrity.

Fabrication of Suspended Ge Nanowires

Properties of tetramethyl ammonium hydroxide (TMAH, $(CH_3)_4NOH$) are well studied especially on orientation dependence of single crystal Si. This chemical solution is also widely applied as Si chemical anisotropic etching solution for advanced nanoscale CMOS manufacture [4]. This study verifies hot TMAH is not only moderate anisotropic etchant for Si [5] but possesses selectivity between Ge and Si. Moreover, TMAH is also effective etchant for defective crystals which is occupied by misfit dislocations (MDs). Fig. 1 illustrates the process flow of Ge NW fabrication. The Si layer is served as seed layer of epitaxial Ge layer (Fig. 1(a)). During the epitaxy process, intrinsic misfit dislocations inhabit near the defective Ge/Si interface which pave sneak path for leakage current in epitaxial GeOI FinFETs. Cl_2 ICP dry etch fabricates fin structures in Fig. 1(b) in following process. TMAH selective etching and H_2O_2 additional etching process is adopted as etchant in Fig. 1(c). 80 ℃ hot TMAH fulfills selectivity between Ge/Si which also eliminates the stacking faults of Ge. This critical recipe provides outright immunity against misfit dislocations and primary leakage by removing defective region to form suspended Ge NWs.After suspended Ge NWs are fabricated, gate stack formation was followed by atomic layer deposition (ALD) to complete NWFETs structure. S/D implantation and activation are accomplished then in gate first process. Fig. 2 shows the perspective view of suspended epitaxial Ge NWFET on SOI substrate. Fig. 3 shows the device characteristics of suspended Ge nNWFET. The electrostatic integrity is significantly improved due to nearly defect free channel region.

Various layout pattern are examined in this study. Fig. 4 shows the cross-sections of Ge NWs on different direction. Due to H_2O_2 solution is used as etchant to narrow down the dimension of nanowires. The oxidation and etch back cycling result in same shape on different direction. Because of various channel direction and nanowire facets, carriers transport in FETs operation behaves different mobility. This is essential for Ge CMOS integration by means of specific pattern design.

Selective etching process is critical in suspended Ge NWs fabrication. It removes Si layer under channel region to blockade leakage path. Leakage current issue interferes CMOS integration especially for Ge device integrated on Si substrate, the situation would be worse due to the Ge/Si misfit defects. Ramped TMAH solution can completely remove Si layer and part of defected Ge/Si interface. This phenomenon realizes the production of suspended Ge NWs and eliminates defected sneaking path full of intrinsic dislocations. Fig. 5(a) shows the cross-section with ICP dry etch only. The intrinsic MDs locates near the Ge/Si interface exaggerate leakage issue. Fig. 5(b) and Fig. 5(c) compare the temperature difference of TMAH solution which also decides the selectivity of etching process for realizing suspended Ge nanowires.

Conclusion

Because of the selective etchant provided by ramped TMAH solution, and dimension scaled down by H_2O_2 solution, we demonstrate nearly defect free suspended Ge NWs on different direction. Ge nNWFETs with superior electrostatic integrity due to elimination of misfit dislocations intrinsically stacked during epitaxy process. This fabrication technique is compatible with CMOS process and beneficial for channel mobility enhancement and circuit design simplicity.

Reference :

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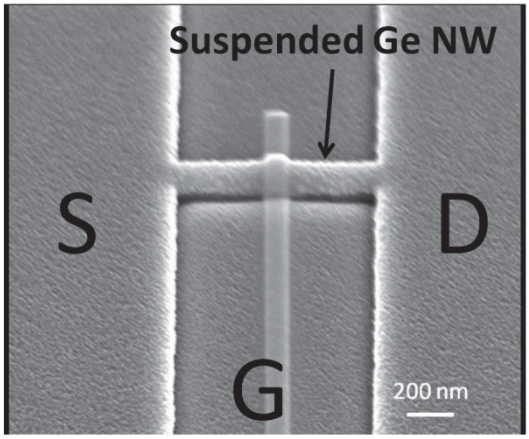

Fig. 2. Tilted SEM image of the fabricated Ge GAA NWFET.

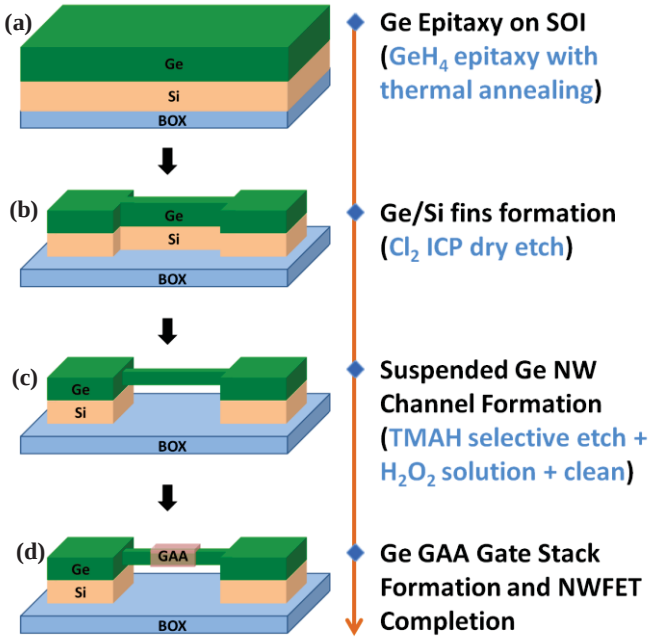

Fig. 1. Process flow of the epitaxial Ge NW grown on SOI substrate with selective etching process.

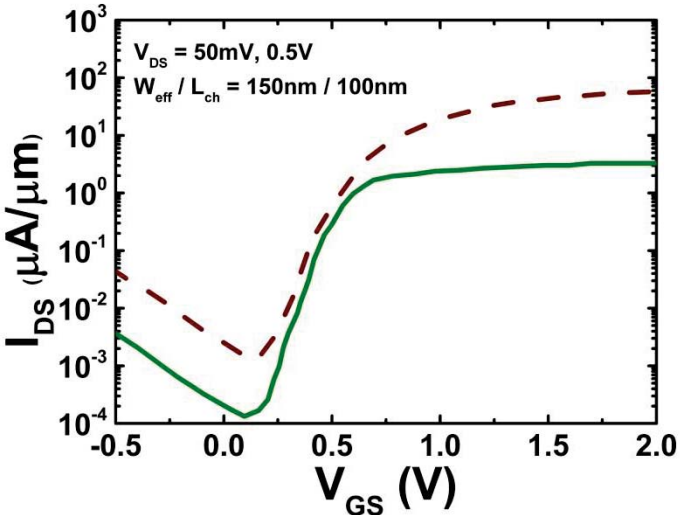

Fig. 3. Transfer characteristics of a Ge NW GAA nFET with selective etching of Ge/Si stack by TMAH solution.

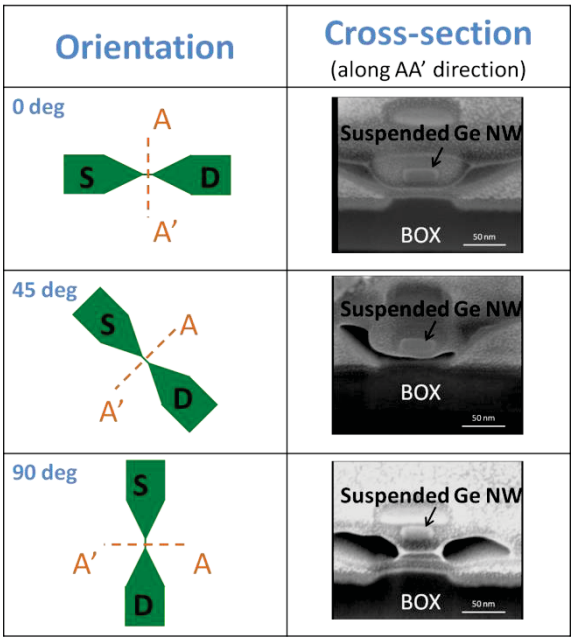

Fig. 4. Cross-section of Ge NWs on different directions.

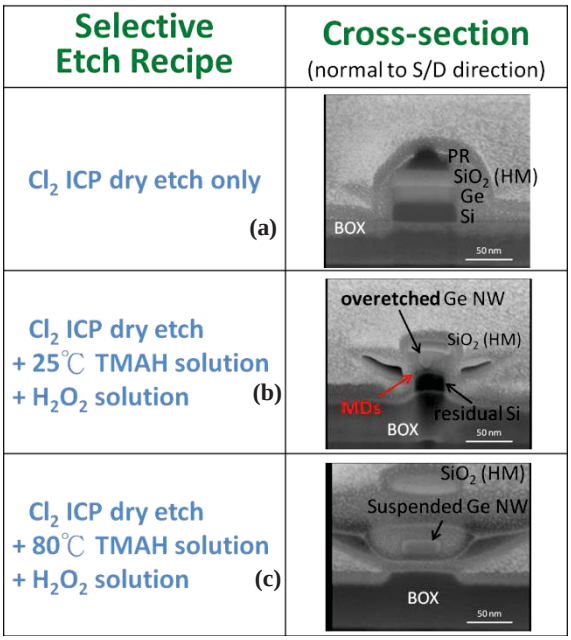

Fig. 5. (a) Ge/Si fin stack fabricated by Cl_2 ICP anisotropic etching. (b) TMAH solution at room temperature shows high etch selectivity of Ge/Si. (c) Hot TMAH solution reveals high etch selectivity of Si/Ge resulting suspended Ge NW formation.