Extended Abstracts of the 2016 International Conference on Solid State Devices and Materials, Tsukuba, 2016, pp229-230

E-1-03

# Impacts on 4H-SiC MOSFET Mobility of High Temperature Annealing in Oxidizing or Inert Ambient before Gate Oxide Growth

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**Abstract**

**The impacts of annealing the substrate before gate oxide formation on 4H-SiC MOSFET mobility were systematically investigated. Annealing the substrate in oxidizing ambient resulted in the degradation of channel mobility, while annealing in inert ambient at high temperature can avoid the degradation. Possible change of substrate surface quality by the introduction of oxygen atoms into the substrate can explain the observed results.**

## 1. Introduction

It has been pointed out that thermal oxidation changes the defect density in 4H-SiC substrate[1], which is considered to be originated from the emission of C and Si atoms from the interface toward substrate[2]. However, the impacts of substrate quality changes during thermal processes on 4H-SiC MOSFET mobility have not yet been clarified. In this study we evaluated channel mobility of 4H-SiC MOSFET subjected to substrate annealing before gate oxide growth, to clarify the effects of substrate annealing in oxidizing or inert ambient.

## 2. Device Fabrication

Lateral n-MOSFETs with various gate length $L_g$ (193 - 448 μm) were fabricated on p-type 4H-SiC (0001) wafers with Al-doped (~$1\times10^{16}$ $cm^{-3}$) epitaxial layers. Source/drain (S/D) regions were formed by phosphorus implantation at 500°C followed by annealing at 1650°C. To investigate the annealing effects in oxidizing ambient, sacrificial oxidations of the substrate before gate oxide growth were conducted at 1300°C in dry-$O_2$ ambient. We controlled the total thickness of sacrificially-oxidized layer of the substrate, as schematically shown in **Fig. 1**. Some of the samples were subjected to annealing in Ar or 1%$H_2$/He ambient at 1150–1500°C after the sacrificial oxidation processes for comparison. Gate oxide of 8–50 nm was formed by thermal oxidation in dry-$O_2$ ambient at 1300°C followed by post oxidation annealing in $O_2$ at 800°C[3]. Metals were deposited onto S/D regions, followed by post metallization annealing at >1000°C in order to form ohmic contact. Finally Al was deposited and patterned as the gate electrode.

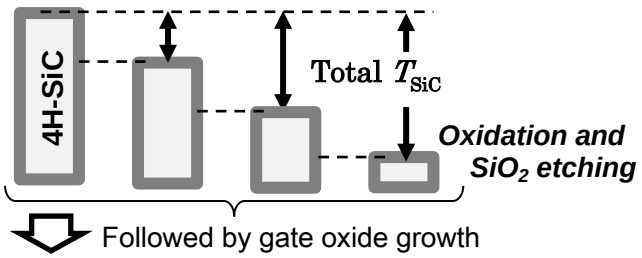


**Fig. 1**. Schematic diagram of consumption of SiC substrate by thermal oxidation and $SiO_2$ etching.

## 3. Results and Discussions

The effects of substrate surface damage by oxidation were investigated by changing the total amount of sacrificial oxidation. The thickness of consumed SiC ($T_{SiC}$) in each oxidation step was estimated from the oxide thickness ($T_{ox}$): $T_{SiC} = T_{ox} / 2.1$. This relationship is derived from that the number of Si atoms in $SiO_2$ is equal to that in consumed SiC substrate. Including the consumption of substrate during the gate-oxide formation, 9–72 nm thick substrate was consumed in total. It was confirmed by using AFM that surface roughness was gradually decreased by those experimental procedures. The field effect mobility ($\mu_{FE}$)-$V_g$ curves for different total $T_{SiC}$ are shown in **Fig. 2(a)**. As a result, a degradation of $\mu_{FE}$ was observed when total $T_{SiC}$

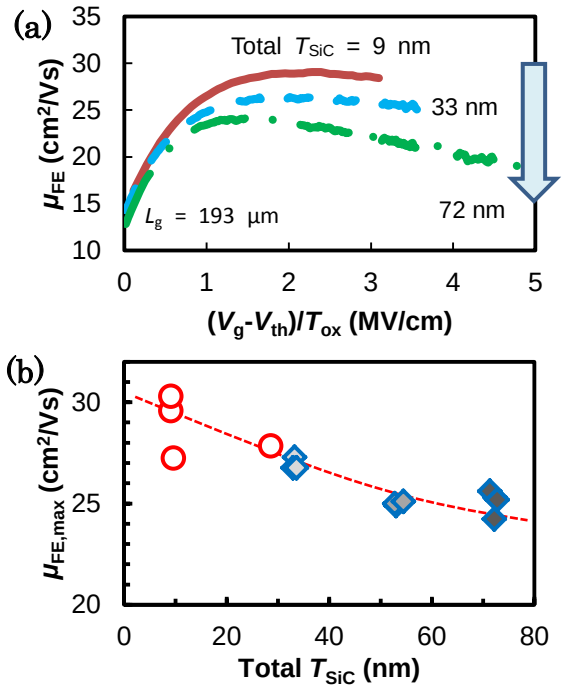


**Fig. 2**. (a) $\mu_{FE}$ -$V_g$ curves of MOSFETs with different total $T_{SiC}$. (b) Total $T_{SiC}$ dependence of maximum $\mu_{FE}$ was extracted. Circles represent the results of MOSFETs without 1650°C activation annealing. Consumption of substrate by oxidation resulted in a reduction of $\mu_{FE}$ in a wide range of gate field.

increased. This clearly indicates that the surface roughness does not always represent the degree of the damage on the substrate surface. To avoid the ambiguity caused by surface damage introduced during activation annealing at 1650°C, we characterized MOSFETs without activation annealing at 1650°C, especially for the region where total $T_{SiC}$ were smaller than 30 nm, as shown by circles in **Fig. 2(b)**. To minimize the errors due to parasitic series resistance in S/D region, we calibrated the results based on the $L_g$ dependence of channel resistance. From above discussions, we can conclude that the thermal oxidation of SiC substrate resulted in a degradation of $\mu_{FE}$.

As the origins of oxidation-induced substrate surface damage, the possible accumulations of C[1], Al[4] and/or O[5] atoms in the substrate by oxidation are suspected. The SIMS analysis (data not shown) hardly detected any accumulation of them, probably due to a relatively high detection limit and its limitation in the analysis of surface part. However, we could observe desorption of oxygen from the substrate, as the form of CO by thermal desorption spectroscopy (TDS) technique. In this experiment, a Si-face wafer was oxidized in $^{18}O_2$ isotope ambient at 1300°C followed by $SiO_2$ etching in HF solution to remove the whole surface oxide before the measurement. As shown in **Fig. 3**, desorption of $C^{18}O$ was clearly observed. Although a quantitation of oxygen density in the substrate was difficult at this moment, the peak intensity suggests the density of oxygen in the substrate was quite larger than theoretically calculated solubility of oxygen[6], which implies the existence of some defects which capture and stabilize the oxygen in the substrate.

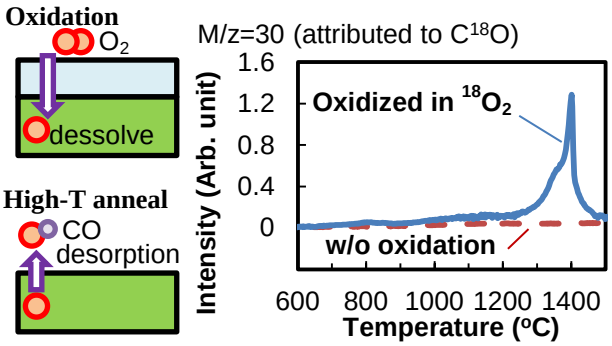


**Fig. 3**. The TDS spectra (M/z=30) of SiC substrate with and without oxidation in $^{18}O_2$ isotope ambient at 1300°C. A clear peak attributed to $C^{18}O$ desorption was detected at ~1400°C, indicating oxygen introduction into the substrate by thermal oxidation.

Also we investigated the effects of substrate annealing without oxygen before the gate oxide growth for comparison. In this experiment, the total $T_{SiC}$ was commonly designed as ~50 nm for every MOSFET. As a result, substrate annealing in diluted-$H_2$ ambient was found to be effective in avoiding degradation of channel mobility, as shown in **Fig. 4 (a)** and **(b)**, which is a clear contrast to the effects of oxidation. Note that the surface roughness was further reduced by annealing even at 1500°C for 60 min, as also shown in **Fig. 4(b)**, suggesting that annealing at 1500°C in inert or reducing ambient do not introduce significant damages on the substrate surface.

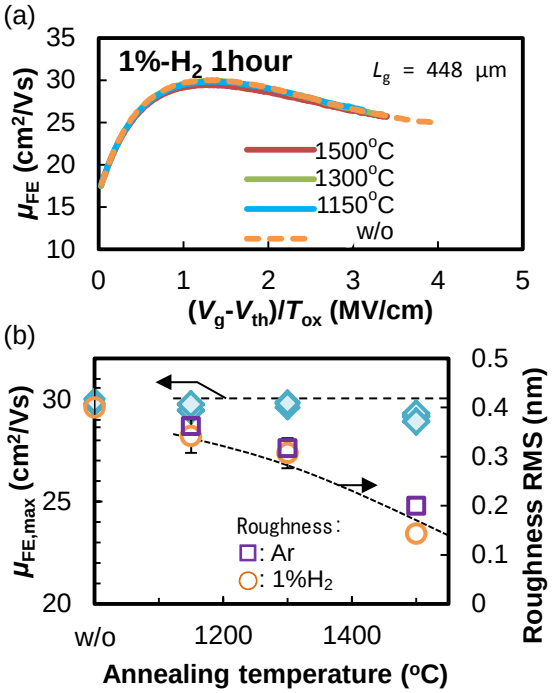


**Fig. 4**. (a) $\mu_{FE}$-$V_g$ curves of MOSFETs subjected to annealing in diluted-$H_2$ ambient at different temperature before gate oxide growth. (b) Maximum $\mu_{FE}$ was extracted. Surface roughness before gate oxide growth is also shown.

## Conclusions

The impacts on 4H-SiC MOSFET mobility of substrate annealing in both oxidizing and inert ambient before gate oxide growth were investigated. Oxidation-induced surface damage mainly originated from the dissolution of oxygen into the substrate, resulted in a degradation of channel mobility. In contrast, high temperature annealing in inert or reducing ambient reasonably avoided the mobility degradation.

**Acknowledgements** This work was partly supported by CSTI, Cross-ministerial Strategic Innovation Promotion Program, "Next-generation power electronics" (funding agency: NEDO), and by JSPS KAKENHI Grant Numbers 26630291 and 15J10704. The TDS measurements were done by Dr. N. Hirashita with ESCO, Ltd. IH-TDS1700.

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