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Reliability Study on Positive Bias Temperature Instability in SiC MOSFETs by Fast I_D Measurement

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Abstract

The gate threshold voltage (V_T) shift under a positive gate bias stress is one of the most important reliability concerns in SiC MOSFETs. Because dynamic recovery is observed as soon as the stress is removed, it is remarkably difficult to accurately determine V_T shifts. In this study, this issue is investigated by introducing a fast measurement technique. In the results, it is found that the time exponents of the V_T degradation are modified to take the V_T recovery term into consideration. It is also revealed that the on resistance (R_{ON}) shows little degradation even if there are large V_T shifts.

1. Introduction

Silicon Carbide (SiC) is an attractive material for high efficiency semiconductor power devices owing to its material properties. However, in n-channel SiC power MOS devices, V_T instability caused by gate bias stress has been one of important reliability issues because SiC MOS interface has many traps from high interface state density. Many studies have focused on this V_T instability issue over the past several years [1-7]. There are two approaches to accurately evaluate the V_T shift: fast measurement [1-4] or calculation from other electric characteristics [5].

Since positive gate bias is applied to operate an n-channel MOSFET, it is considered that positive bias temperature instability (PBTI) is a more important issue. Thus in this study, we investigated V_T shifts and recovery behaviors in PBTI stress by using a fast or nonfast measurement technique.

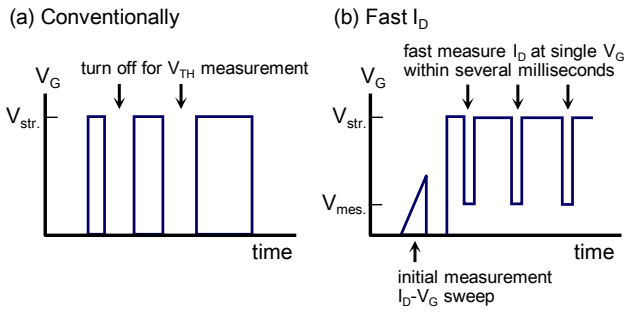

Fig. 1 Schematic sequences of gate bias in PBTI tests: (a) conventional method interrupts gate bias for measurement, (b) Fast I_D method dumps gate with no turn-off time [8-9].

2. Experiments

In this study, we used 1.2 kV three terminal n-channel SiC DMOSFETs. The samples were fabricated on an (0001) Si faced 4H-SiC n-type epitaxial layer with an n-type substrate. The key MOS gate structure was formed in dry oxygen ambient. After forming thermal SiO_2 films with a thickness of 50 nm, NO nitridation annealing and other treatments were performed to reduce the interface state density.

We evaluated PBTI phenomena in SiC MOSFETs by using the Agilent B1505 parameter analyzer. We introduced two types of PBTI test methods, as shown in Fig. 1. In the nonfast conventional method, the gate voltage stress is interrupted for I_D-V_G measurement for at least several seconds. This stress-off time possibly causes V_T recovery in SiC MOSFETs. On the other hand, the Fast I_D method is a major and standard technique to evaluate negative bias temperature instability (NBTI) in p-channel Si MOSFETs, which is an important reliability concern in submicron CMOS processes [8-9]. The Fast I_D method measures I_D at dumped single V_G points as fast as possible with no stress-off time. If measuring points are in a linear region, V_T shifts (ΔV_T) are calculated from I_D shifts and the initial g_m, shown in eq. (1):

$$\Delta V_T(t) = \frac{I_D(0) - I_D(t)}{g_{m(max)}(0)} \quad . \qquad (1)$$

3. Results and Discussion

Fig. 2 compares the V_T curves before and after PBTI stress for the same SiC MOSFET sample. The applied PBTI stress is $V_G = 20$ V for 1000 s at 20 °C. The V_G-I_D curve shows a positive shift for V_G stress; moreover, the shift is parallel. This is an important result because ΔV_T is calculated by using the initial g_m in the Fast I_D method. Therefore, g_m, which is the slope of the V_G-I_D curve, should be time independent to apply the Fast I_D method.

Fig. 3 shows V_T shifts as the results of PBTI tests. The V_T shifts in low temperature are larger than that in high temperature. This is understood by slow detrapping and channel mobility temperature characteristic. However, time exponents are not the same value, increasing V_T data plots are described by power law functions. The reason the conventional method gives a relatively large time exponent is considered to be a lack of the recovery term in an analogy of the NBTI issue.

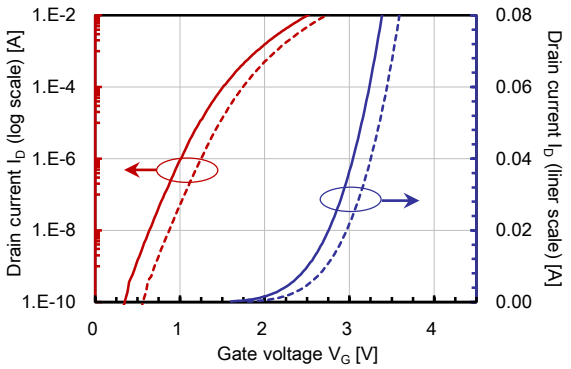

Fig. 2 I_D-V_G characteristics before (solid lines) and after (dotted lines) PBTI stress (T_j = 20 °C, V_G = 20 V, 1000 s) for the same SiC MOSFET sample.

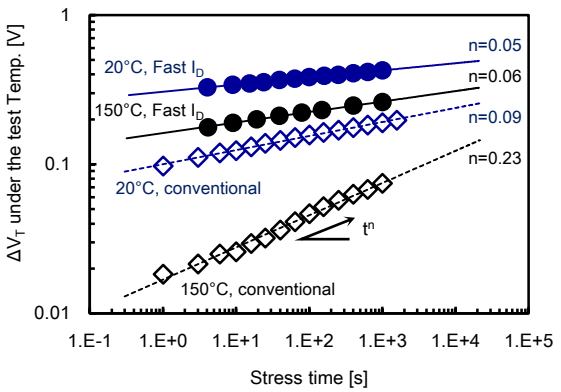

Fig. 3 V_T shifts versus PBTI stress time by two measurement methods. Stress voltages were V_G = 20 V.

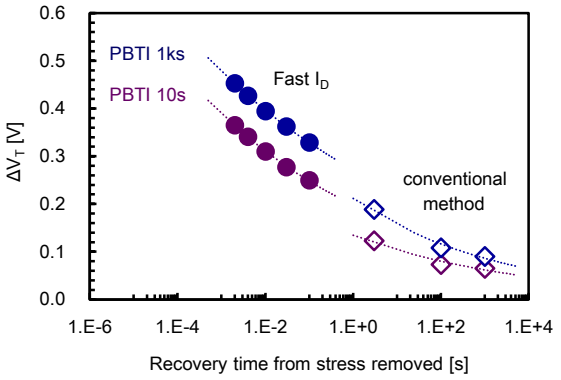

Fig. 4 V_T recovery behaviors after PBTI stress is removed. The PBTI conditions are T_j = 20 °C, V_G = 20 V, 10 s or 1000 s.

The V_T recovery data is shown in Fig. 4. Once the PBTI stress is removed, V_T recovery is observed. Fast I_D evaluates with a measuring delay of milliseconds, although the conventional method catches almost recovered values, shown in Fig. 4. Comparing PBTI stress data at 10 s and 1000 s, the recovery speed seems to have almost no time dependence within a few seconds. Consequently, almost fixed recovery terms reduce their power law time exponents in the Fast I_D method, as

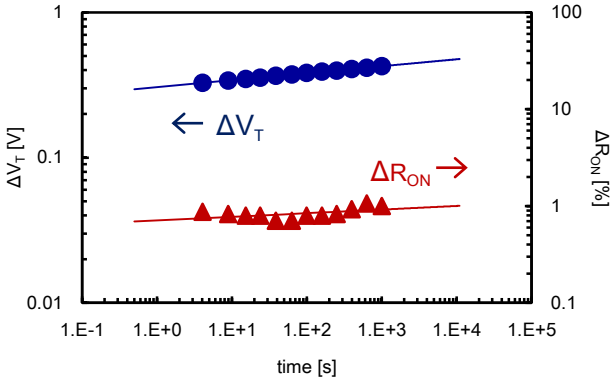

Fig. 5 V_T and R_{ON} shifts versus PBTI stress time (T_j = 20 °C, V_G = 20 V, Fast I_D). V_G = 18 V for R_{ON} measurement.

shown in Fig. 3. The gap of time exponents between the conventional method and the Fast I_D method tends to be crucial in higher-temperature conditions. In addition, the plots shown in Fig. 4 do not appear to be fitted in a single line. This is because Fast I_D has no turn-off time in measuring I_D to calculate the V_T shift. Therefore, the plots of Fast I_D do not indicate strict recovery behaviors.

R_{ON} is one of the most important electric characteristics in power devices. Fig. 5 shows the R_{ON} shifts in PBTI tests. It is clear that R_{ON} shifts are within 1% from the initial value even though V_T shifts are large. To measure R_{ON}, it is necessary to apply sufficient gate bias (in this case, V_G = 18 V) to open the MOS channel fully. Consequently, the following two mechanisms can be considered: an initial R_{ON} value has already been degraded by the on-gate bias, and the high-density on-current is insensitive to trapped charges. Thus, it is expected that large R_{ON} shifts are not observed in general usage.

4. Conclusions

We investigated the V_T instability of SiC MOSFETs in PBTI. SiC MOSFETs show large V_T shifts and fast recovery behaviors after the PBTI stress is removed. We explained the V_T degradation by using a power law time exponent. Time exponents differ depending on measurement methods. However, V_T is so sensitive to the gate bias stress, it was also found that R_{ON}, which is one of the most important characteristics for power MOSFETs, shows relatively small shifts compared with those of V_T.

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