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Positive Bias Temperature Instability of SiC-MOSFETs Induced by Switching Operation (AC-PBTI)

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Abstract

Despite the advances in SiC-MOSFET technology in recent years, high temperature stability remains a significant issue. In this work, we report on the positive bias temperature instability of SiC-MOSFETs induced by gate-switching operation (AC-PBTI). The dependence of ΔV_{th} on the duty-cycle of the gate-pulse is measured, and shows strong dependence on off-voltage, which has not been reported in previous studies on-Si-MOSFET BTI. The well-known trap-detrap model for Si is used to explain this abnormal behavior.

1. Introduction

SiC-MOSFETs have attracted attention as a key device for future power electronics. However, their high- temperature stability has been discussed intensively as a major reliability issue [1]. Fast measurement results have also been reported to detect fast recoverable components [2, 3].

In Si-LSIs, AC-BTI has been thoroughly studied for more than 10 years by taking into account the CMOS circuit operation [4]. Thus, the switching operation should be examined in relation to the BTI of power MOSFETs. For example, in DC-DC converter applications, the duty-cycle (d) dependence and effect of negative gate-bias as off-voltage $V_{gs}(OFF)$ are very important in estimating the effect of BTI on the power circuit operation.

In the present work, AC-stress measurement results for SiC-MOSFETs obtained by using several AC-stress patterns are reported for the first time. These results are discussed on the basis of the trap-detrap model [5], which has been proposed to explain the recoverable component of BTI for Si-pMOSFETs.

2. Experimental

Commercially available 3-terminal SiC-MOSFETs were measured and stressed by using a Keysight B2902A source measure unit [6]. An AC-stress voltage of 1 KHz with various duty-cycles and gate off-voltages is applied.

3. Results and Discussion

Degradation and Recovery of I_{ds}-V_{gs} Characteristics by DC-PBTI

Figure 1 shows the shift in threshold voltage (V_{th} is defined at I_{ds}=1E-5A) during PBT stress at 200℃. A clear power-law time-dependence is observed for V_{gs}=20V-35V. ΔV_{th} is mainly positive, which suggests electron-trapping in the oxide. Sweep measurement (0-25 V) was carried out; thus, the fast recoverable component is omitted. However, the fast measurement suggests that the contribution of this component becomes relatively small at 200℃ [2]. This power-law is familiar in studies on Si BTI [4].

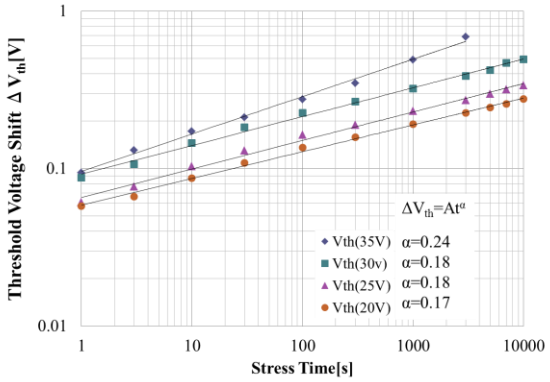

Fig. 1 Time-dependent ΔV_{th} of the SiC-MOSFETs during PBT stress (DC stress: 20-35V, 200℃; sweep :0-25V).

Figure 2(a) shows an example of recovery behavior at V_{gs}=-10 V. The stress voltage is V_{gs}=35V. A large amount of the change in I_{ds}-V_{gs} characteristics can be recovered within 1 sec. Another sample showed faster recovery at V_{gs}=-5 V after 30V stress, as measured by a faster measurement method to monitor I_{ds} (Fig. 2(b)). These behaviors can be attributed to the trapping and detrapping of electrons to and from preexisting electron traps.

It should be noted that the observed negative ΔV_{th} for V_{gs}=-5 V is probably due to additional hole trapping, which has been clearly observed in FN stress experiments [6]. Thus, V_{gs}=30V stress has some components of FN stress, causing FN tunneling and hot carrier generation, which result in hole trapping.

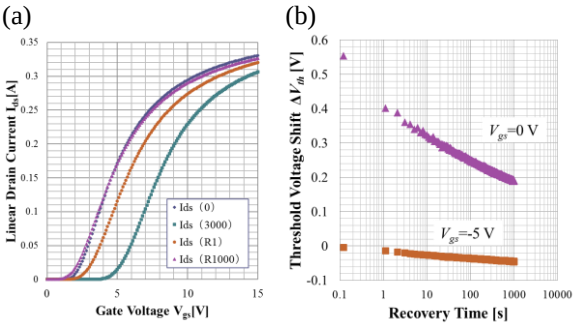

Fig. 2 (a) Linear I_{ds}-V_{gs} characteristics (sweep:0-25V) of the SiC-MOSFET during PBT stress (35V, 200℃) and recovery (-10 V, 200 ℃). (b) Time-dependent recovery of V_{th} of the SiC-MOSFET (stress: 30 V, 200℃; recovery: 0 or -5 V, 200℃; ΔV_{th} : estimated by spot I_{ds} measurement).

AC-PBTI of SiC-MOSFETs

The duty-cycle dependence of ΔV_{th} for V_{gs}*(OFF)*=0V and -5V is presented in Fig. 3. The large difference between the two conditions is striking, although this finding agrees well with the recovery data shown in Fig. 2(b). Since the electron traps are located at near-interfacial region (<1 nm, [6]), the difference in the electron tunneling probability seems very small. An expected large change in the band bending between 0V to -5V could be the cause of this phenomenon.

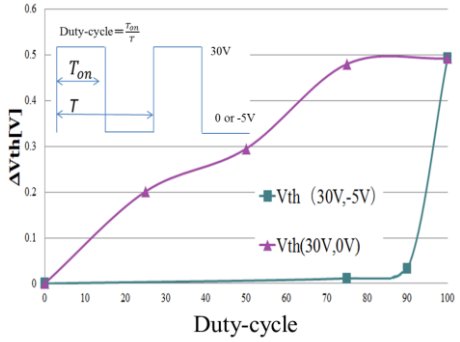

Fig. 3 Duty-cycle dependence of ΔV_{th} (sweep:0-25V) of the Si-MOSFET during AC- PBT stress (30V, 200℃, 1 KHz).

Trap-detrap model for near-interfacial electron traps

In studies on Si-LSI BTI, the trap-detrap model is well known for N_{ot} formation [5] and the reaction-diffusion model for N_{it} formation [4]. We apply this trap-detrap model to the AC-PBTI of SiC-MOSFETs. The following rate equations are used for the electron occupation probability of electron traps in the oxide:

$$\frac{df_s(t)}{dt} = \frac{1}{\tau_c}\left[1 - f_s(t)\right] \quad \text{:ON(stress)} \qquad (1)$$

$$\frac{df_r(t)}{dt} = -\frac{1}{\tau_e} f_r(t) \quad \text{:OFF(recovery)} \qquad (2)$$

The exact solution can be obtained [7] and can explain the oscillatory behavior reported very recently [3]. Figure 4(a) shows the simulation results of an equivalent RC circuit [5], obtained by using the LTspice software.

In the high-frequency limit, the following coarse-grained equation (3) and its solutions (4)(5) are useful as shown in Fig. 4 [7]:

$$\frac{df_{CG}}{dt} = \frac{d}{\tau_c} - \left(\frac{d}{\tau_c} + \frac{1-d}{\tau_e}\right) f_{CG} \qquad (3)$$

$$f_{CG}(t) = f_{sat.}\left(1 - e^{-\frac{t}{\tau_{CG}}}\right) + f(0)e^{-\frac{t}{\tau_{CG}}}, \quad \frac{1}{\tau_{CG}} \equiv \frac{d}{\tau_c} + \frac{1-d}{\tau_e} \qquad (4)$$

$$f_{sat.} \equiv f_{CG}(\infty) = \frac{1}{1 + \frac{\tau_c(1-d)}{\tau_e d}} \qquad (5)$$

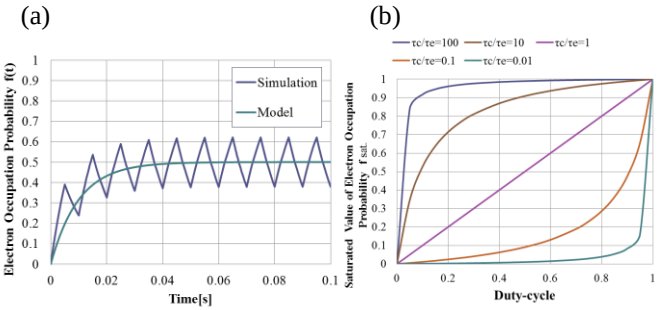

Fig. 4 (a) Results of the simulation and Eq. (4) of the rate equations (1)(2). (b) Duty-cycle dependence of the saturated value of electron occupation probability of electron traps in the oxide (Eq. (5)).

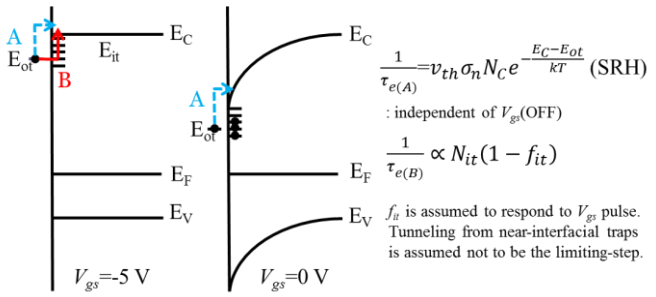

Fig. 5 Band structure showing the possibility of interface-states assisted detrapping of electrons, which is effective under V_{gs}=-5 V.

The duty-cycle dependence of $f_{sat.}$ relies on the ratio τ_c/τ_e. This model suggests that $\tau_e(V_{gs}$=-5 V)<<$\tau_e(V_{gs}$=0 V) in our observation (Fig. 3). However, the emission probability by the SRH mechanism is independent of E_F, which is determined by V_{gs}(OFF) [8]. Thus, another mechanism should be considered. Figure 5 shows a new interface-states assisted detrapping model. The tunneling probability of trapped electrons in the oxide toward the interface states is proportional to the non-occupation probability of electrons in the states, 1-f_{it}, which is a strong function of E_F. As a result, V_{gs}=-5 V leads to a very small τ_e.

4. Conclusions

From the duty-cycle dependence of the AC-PBTI of SiC-MOSFETs, a small negative V_{gs}(OFF)=-5V is shown to enhance the electron detrapping from the near-interfacial oxide traps. A large change in band bending between 0V to -5V could be the cause of this phenomenon. The interface-states assisted detrapping mechanism is proposed.

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