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Advanced 1.2 kV Class SiC MOSFETs Fabricated on 150 mm wafers in a High-volume CMOS Fab

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Abstract

Design and manufacturing process for high-voltage SiC MOSFETs have been developed in a 150 mm CMOS fab. 1.2 kV class MOSFETs have been fabricated on this production line running in parallel with CMOS wafers. Typical devices have state-of-the-art performance with specific on-resistance of 4.5 milliohm-cm^2 and low leakage current up to 175^{O}C junction temperature. The process manufacturability and quality of 150 mm SiC wafers have been verified by running multiple lots with consistent results. Manufacturing rugged 1.2 kV SiC MOSFETs in high-volume 150 mm CMOS fab can disrupt cost and reliability barriers of SiC MOSFETs and drive wide spread adoption.

1. Introduction

Silicon carbide power MOSFETs can reduce the cost and increase the performance of power electronics systems but devices must be delivered that provide not only the required performance, but also the necessary cost and reliability. One approach to achieve this is to manufacture SiC MOSFETs in a high-volume, automotive qualified 150 mm silicon CMOS fab reusing well understood silicon processes. We have developed design and process techniques to fabricate high-performance, 1.2 kV SiC power MOSFETs on 150mm SiC wafers in a high volume silicon CMOS production line [1]. CMOS processes have been integrated with SiC MOSFET process flow and both silicon and SiC wafers run in parallel with no interruption to the production line. To the best of our knowledge, this is the first demonstration of manufacturable and robust SiC MOSFETs from a high-volume 150mm CMOS fab that can disrupt cost and reliability barriers of SiC MOSFETs and drive wide spread adoption.

2. Design, Fabrication and Results

Device Design

To achieve a rugged SiC MOSFET, it is critical to ensure stable and uniform avalanche in the device unit cells and avoid high fields in the oxide or breakdown in the termination. The device termination designed in this work achieves close to ideal parallel plane breakdown voltage (BV) over a wide dose range providing a wide process margin. Besides the device termination, the JFET region of the device under oxide needs to be optimized to minimize on-resistance and oxide field under high voltage reverse bias stress. The device is designed such that the device always breaks down at center of the unit cell ensuring uniform avalanche and low peak field in the oxide. Other critical aspects of the device and process design are optimizing the channel and P-well design to ensure that the device remains off over entire voltage and temperature envelope. The MOSFET designed in this work combines all these aspects resulting in a rugged design with wide process margin.

Fabrication process

Primary roadblocks in processing SiC wafers in a CMOS fab are requirement of high temperature processing and handling semi-transparent wafers. Other challenges are process integration of CMOS steps and SiC-specific process steps. All metal and dielectric stacks have to be compatible with a standard CMOS fab. Monolith's SiC MOSFET process was developed with these constraints in mind. Standard process steps available in a CMOS foundry were reused wherever possible; examples include implant masking steps, top level interconnects. SiC-specific processes were developed using CMOS production tools for certain steps like contacts, gate oxidation among others. Only steps for which special SiC-specific tools were used are implant activation and certain ion implantation steps. Mechanical wafer handling had to be modified or optimized for a number of process steps due to semi-transparent nature of SiC and different wafer thickness compared to 150 mm silicon wafers. This approach ensured that the SiC wafers can be run in parallel with the silicon wafers in high volume production taking full advantage of low cost and automotive qualified production processes running in the CMOS fab.

Results

1200V, 65milliohm MOSFETs have been fabricated in multiple wafer lots with various process and design splits and characterized both at wafer level and in TO-247 packages. Fig. 1 shows typical off-state IV (V_{gs}=0) characteristics of fabricated MOSFETs from 25^{o}C to 175^{o}C with low leakage current (<100uA) over worst case voltage and temperature envelope. On-state IV of these MOSFETs at 25^{o}C is shown in Fig. 2. Typical on-resistance of these MOSFETs at V_{gs}=20V, 25^{o}C is 65 milliohm and increases to 125 milliohm at 175^{o}C. While these devices are particularly optimized for robustness and manufacturability, typical specific on-resistance is 4.5 milliohm-cm^2, competitive with commercially available 1.2 kV SiC MOSFETs. With more aggressive process and designs, specific on-resistance of 3.1 milliohm-cm^2[1] has been achieved on the same process platform.

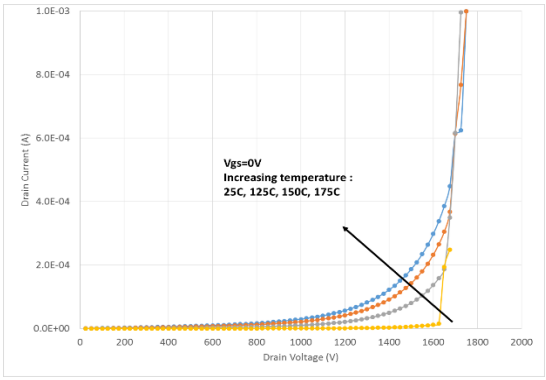

Figure 1 : Typical off-state IV characteristics (V_{gs}=0) for temperatures 25°C to 175°C.

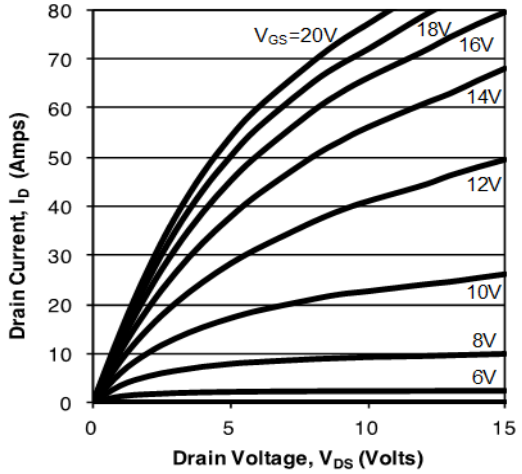

Figure 2 : Typical on-state IV characteristics at 25°C. On-state resistance=65 milliohm.

In order to achieve low cost, it is imperative that the process is manufacturable with sufficient margin. 150 mm SiC wafers are relatively new entrants to the market compared to 100 mm wafers. Defect density of 150 mm SiC wafers were investigated with yield of diode leakage current with similar die size. High yields of >90% and random spatial distribution confirmed high quality of 150 mm wafers [2]. One aspect of the process that needs improvement is the epitaxial doping control of 150 mm wafers. State-of-the-art wafers result in wider BV distribution than desirable. The process has been designed to accommodate this and has sufficient BV margin. Large quantity of devices from multiple wafers manufactured in different fab lots have been characterized to confirm excellent manufacturability [2].

Reliability of the devices has been studied with various stress tests. Gate oxide was studied with TDDB and Qbd tests, threshold voltage stability with HTGB test at 175°C with positive and negative gate bias and high-voltage reliability with HTRB at 175°C [1,2,3]. Of particular significance is the result presented in [3], which compared the quality of the SiC MOS capacitors manufactured with this process with high quality silicon capacitors.

The MOSFETs have also been characterized for avalanche energy and short circuit withstand capability to investigate the ruggedness of the devices. Avalanche energy of the devices has been showed to be greater than 1 Joule at 20A avalanche current and the devices can withstand longer than 5 microsecond short-circuit condition with V_{ds} of 800V and V_{gs} of 20V. Statistical distribution for these numbers are under investigation.

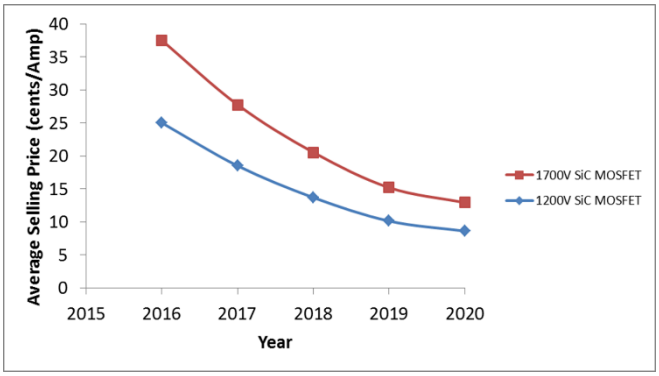

Figure 3 : Projected normalized average selling price (cents / Amp) of 1200V and 1700V SiC MOSFETs over next 5 years.

Final frontier for widespread adoption of a new technology is the cost. Based on forward looking estimates of wafer price, processing price, device yields, we have projected normalized average selling price of 1200V and 1700V SiC MOSFETs over next few years. This calculation also assumes a 50% gross margin. While the absolute numbers depend on various conditions, these curves predict a significant cost reduction of SiC MOSFETs over next 5 years compared to current market price.

3. Conclusions

In summary, we have developed 1.2 kV SiC MOSFETs in a high-volume, automotive-qualified 150mm CMOS line. These MOSFETs have state-of-the-art performance with excellent manufacturability, ruggedness and reliability up to 175°C. These characteristics can disrupt cost and reliability barriers of SiC MOSFETs and drive wide spread adoption.

Acknowledgements

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