

Threshold voltage control of organic thin film transistors (OTFTs) by using floated double gate structure

Sunghoon Lee, Tomoyuki Yokota and Takao Someya

Department of Electrical Engineering, University of Tokyo

7-3-1 Hongo, Bunkyo-ku, Tokyo, 113-8656, Japan

Abstract

We demonstrated a novel transistor structure comprising a floated electrode and a double gate electrode. The floated double gate structure showed a linear V_{TH} controllability after the transistor fabrication without performance degradation. The numerical calculation was performed for the mobility estimation and it showed a good agreement with the experimental results.

1. Introduction

Organic electronics have been developed due to inherent material properties such as flexibility, lightweight, and printability. Threshold voltage (V_{TH}) is one of important transistor parameters as it determines the design and performance of circuits. V_{TH} has been controlled by various methods, including the floating gate structure [1], the double gate structure [2], the surface modification of dielectric layer, such as the plasma irradiation [3] or self-assembled monolayers(SAMs) [4], and the work function control of the gate electrode [5]. Post-fabrication controllability is preferable because it enables not only to compensate the change of V_{TH} due to unstable behavior of OTFTs but also to realize uniform OTFTs for the circuits.

In this work, we proposed the novel structure which combines both the floating gate and the double gate for post fabrication control. The linear V_{TH} controllability was demonstrated without degrading other transistor performances.

2. Experimental results

2.1 Fabrication of the floated double gate transistors

A schematic of a transistor is shown in Fig. 1. First, a 50 nm thick Au was thermally evaporated on a 75 μm thick polyimide substrate with a shadow mask. A 60 nm-thick parylene layer was deposited as a first gate dielectric layer where the parylene was deposited by the chemical vapor deposition (CVD) method. Subsequently a gold layer was formed for a floated electrode and the second parylene dielectric was deposited. A dinaphtho [2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT) was thermally evaporated as an organic semiconductor layer. Finally, a 60 nm-thick gold layer was evaporated as source/drain electrodes. Simultaneously, the double gate electrode was deposited on the 2nd parylene and the floated electrode. The length and width of the channel are 36 μm and 500 μm , respectively. Here, the voltage of the floated electrode (V_{FG}) is determined by electrostatic

potential balance between the bottom gate electrode and the double gate electrode. The capacitance ratio was varied by using the different area of the double gate electrode. The bottom gate capacitance C_{BG} , which is the capacitance between the floated electrode and the bottom gate, is designed to be 392.2 pF. The double gate capacitance C_{DG} , which is the capacitance between the floated electrode and the bottom gate, is designed to be 42.0 pF (case 1) or 126.0 pF (case 2). The fabricated transistors are shown in Fig. 2.

2.2 V_{TH} controllability of the floated double gate structure

Figure 3 (a) shows the drain current-bottom gate voltage (I_D - V_{BG}) characteristics with the various double gate voltages (V_{DG}) from -10 V to 10 V and the capacitance ratio of 0.107 (case 1). Constant drain voltage of -5 V was applied. By varying the double gate voltage, we were able to control the V_{TH} , without degradation in the off current, the subthreshold swing, and the mobility. The off currents were maintained less than 10 pA at VBG from -5 V to 5V. By increasing the V_{DG} , the transfer curve showed a positive shifting which reflects the potential change of V_{FG} by V_{DG} . The V_{TH} was plotted as a function of V_{DG} in Fig. 3 (b). V_{TH} was -0.13 V when -10 V applied to V_{DG} . V_{TH} showed linear increment as increasing V_{DG} . The V_{TH} change by V_{DG} could be explained by the analysis of the electrostatic potential.

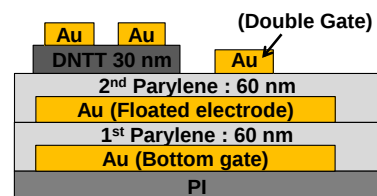


Fig. 1 A schematic of the cross-section of the floated double gate transistor

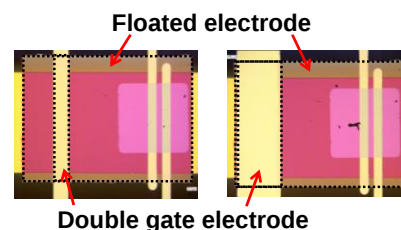


Fig. 2 Optical images of fabricated transistors with small double gate electrode (left, case 1) and large double gate electrode (right, case 2)

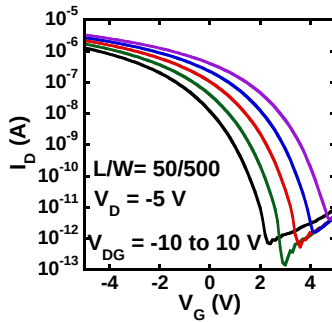
The controllability was simply determined by the capacitance ratio between C_{DG} and C_{BG} , since V_{FG} is determined by the dominance of each electrode. With the small double gate electrode (case 1), the capacitance ratio was 0.107 and it is similar with the present slope (0.149) of V_{TH}/V_{DG} . With the large double gate electrode (case 2), the capacitance ratio was 0.321 and the slope of V_{TH}/V_{DG} is 0.366. In other words, the strong V_{TH} controllability could be achieved easily by increasing the area of the double gate electrode and it is not necessary to control the thickness of the dielectric layer. However, the large double gate electrode makes the dominance of the bottom gate electrode weak in the channel. The saturation current of the floated double gate transistor could be described as

$$I_D = \frac{1}{2} \frac{W}{L} C_{CHN_FG} (V_{FG})^2$$

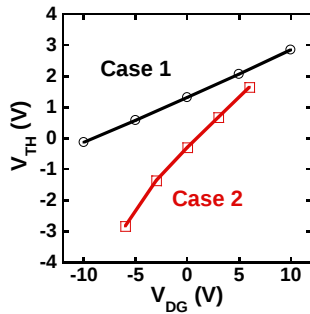
where W is the channel width, L is the channel length, C_{CHN_FG} is the capacitance between the floated electrode and the channel of the semiconductor, V_{FG} is the voltage of the floated electrode. The effect of V_{TH} was ignored for simplicity. The C_{CHN_FG} was not affected by the structure. However, the effective capacitance of the bottom gate was changed by the design and the structure. The relation between V_{FG} and V_{BG} should follow the equation as below under the accumulated status.

$$V_{FG} \propto \frac{C_{BG}}{C_{BG} + C_{DG} + C_{OSC} + C_{SD}} V_{BG}$$

Here C_{OSC} is the capacitance between the DNTT layer and the floated electrode and C_{SD} is the capacitance between the source/drain electrodes and the floated electrode, which are not located above the DNTT layer.



(a)



(b)

Fig.2 (a) Transfer curves with various double gate voltages (b) V_{TH} versus the double gate voltage with different capacitance ratio

Therefore, the drain current is expressed as below.

$$I_D = \frac{1}{2} \frac{W}{L} C_{CHN_FG} \left(\frac{C_{BG}}{C_{BG} + C_{DG} + C_{OSC} + C_{SD}} \right)^2 (V_{FG})^2$$

As results, the apparent capacitance (C_{CHN_BG}) between the bottom gate electrode and the channel is $C_{CHN_FG} (C_{BG}/(C_{BG}+C_{DG}+C_{OSC}+C_{SD}))^2$. Here, C_{CHN_FG} is 46.7 nF/cm², C_{BG} is 392.2 pF, C_{DG} is 42.0 (case 1) or 126.0 (case 2) pF, C_{OSC} is 116.7 pF, and C_{SD} is 52.3 pF. The C_{CHN_BG} of the case 1 and case 2 are 19.4 nF/cm² and 14.9 nF/cm², respectively. The mobilities are plotted as a function of V_{DG} in Fig. 3. Even in various V_{DG} , a stable and constant mobility was achieved. Similar mobilities with various C_{DG} were recorded by considering the effective capacitance. The apparent capacitance of the bottom gate electrode, V_{TH} controllability, and the designed capacitance are summarized at Table 1.

3. Conclusions

In summary, we demonstrated the novel transistor structure comprising the floated electrode and the double gate electrode. The floated double gate structure showed V_{TH} controllability after the transistor fabrication without performance degradation of transistors. Numerical calculation was performed for the mobility estimation and it showed a good coincidence with experimental results.

Acknowledgements

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References

1. T. Yokota, et al., *Appl. Phys. Lett.*, vol. 98, p. 193302, 2011
2. S. Iba, et al., *Appl. Phys. Lett.*, vol. 87, p. 023509, 2005
3. A. Wang, et al., *Appl. Phys. Lett.*, vol. 89, p. 112109, 2006
4. U. Zschieschang, et al., *Adv. Mater.*, vol. 22, pp. 4489, 2010
5. R. Shiwaku, et al., *Appl. Phys. Lett.*, vol. 106, p. 053301, 2015

Table. 1

	C_{DG} (pF)	C_{BG} (pF)	C_{DG}/C_{BG}	V_{TH}/V_{DG}	C_{CHN_BG} (nF/cm ²)
Case 1	42.0	392.2	0.107	0.149	19.4
Case 2	126.0	392.2	0.321	0.366	14.9

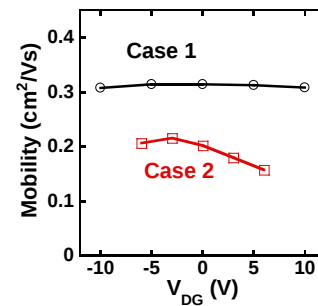


Fig.3 Mobility versus the double gate voltage with different capacitance ratio