Extended Abstracts of the 2016 International Conference on Solid State Devices and Materials, Tsukuba, 2016, pp269-270

F-1-05

Low voltage operation of organic n-type thin film transistor with solution process.

Kuribara Kazunori[1], Shunsuke Aoki[2,†], Kazuaki Kakita[3], Yasuhiro Tanaka[3], Takehito Kozasa[1], Sei Uemura[1], Taiki Nobeshima[1], Takeshi Kawai[2] and Manabu Yoshida[1]

[1] National Institute of Advanced Industrial Science and Technology (AIST)
1-1-1 Higashi, Tsukuba, Ibaraki, 305-8565, Japan
Phone: +81-29-861-4536 E-mail: kuribara-kazunori@aist.go.jp
[2] Tokyo Univ. of Science
1-3 Kagurazaka, Shinjuku-ku, Tokyo 162-8601, Japan
[3] Ube industries co., Ltd.
Seavans North Building, 1-2-1, Shibaura, Minato-ku, Tokyo 105-8449, Japan
† present address: Japan Advanced Institute of Science and Technology (JAIST)
1-1 Asahidai, Nomi, Ishikawa 923-1292 Japan

Abstract

We have investigated solution process of organic n-type thin film transistors (TFTs). We use novel benzo-bis(thiadiazole) derivative as n-type semiconductor, and choose push coating method to form semiconductor layer on hydrophobic gate dielectric which enables low voltage operation below 6 V. In this study, we have optimized temperature and time during push coating. TFT with this flat semiconductor film shows mobility of 0.06 cm^2/Vs. Subsequently, we have patterned that semiconductor by reverse offset transfer method. Finally, TFTs with patterned semiconductor film shows mobility of 8×10^{-4} cm^2/Vs with on/off ratio of 10^3 at operation voltage of 2.5V.

1. Introduction

Recently, organic/flexible electronics have been intensively studied in variety field. High mobility n-type material is one of the large concern for organic electronics. Many novel materials are reported today [1][2]. However almost all materials requires alkyl halides or some kind of organo halides. Some benzobis(thiadiazole) derivative named TU-1 is reported as a solution processable material and shows high mobility of 0.56 cm^2/Vs[3]. We improve its solubility for other solvent without halides, and form semiconductor thin film by solution process. In addition to that, we simultaneously reduce operation voltage from several tens voltages up to 2 V for actual use. To reduce operation voltages, many pioneer researchers have developed high capacitive gate dielectrics [4][5]. In this study, we have chosen self-assembled monolayer (SAM) as gate dielectrics. This quite thin insulator film requires only easy solution process and low temperature process below 100 deg.C [6]. It suits flexible substrates. However, surface of SAM is hydrophobic and it is difficult to form organic thin film on it with solution process.

Objective of this study is to form n-type material named TU-2, which is improved from TU-1 on solubility, onto hydrophobic surface and to realize high mobility and low operation voltage, simultaneously, with push coating method [7]. In the next step, we try to make pattern of semiconductor by reverse offset transfer and verify inverter operation.

2. Experimentals

Fabrication process

We fabricated organic transistor with solution process and thermal deposition process. Fig. 1 shows schematic structure of transistor. At first, we deposited aluminum layer onto

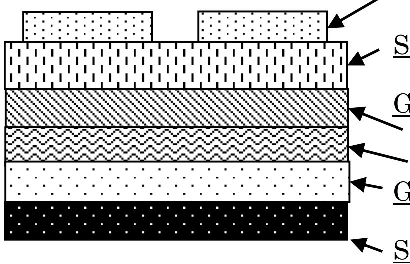

Fig. 1 Schematic TFT structure. Semiconductor layer is formed with two ways. One is direct push-coating and the other is transfer of push-coated film by reverse offset transfer.

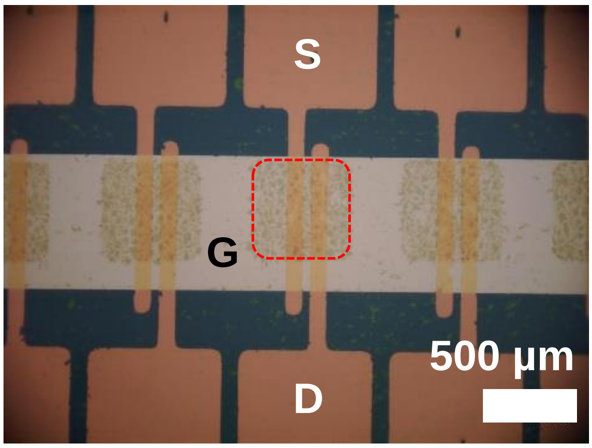

Fig. 2 Photo of TFT with patterned TU-2 film. Patterned semiconductor is transferred onto hydrophobic SAM gate insulator. Broken red square shows TU-2 film. Scale bar describes 500 µm.

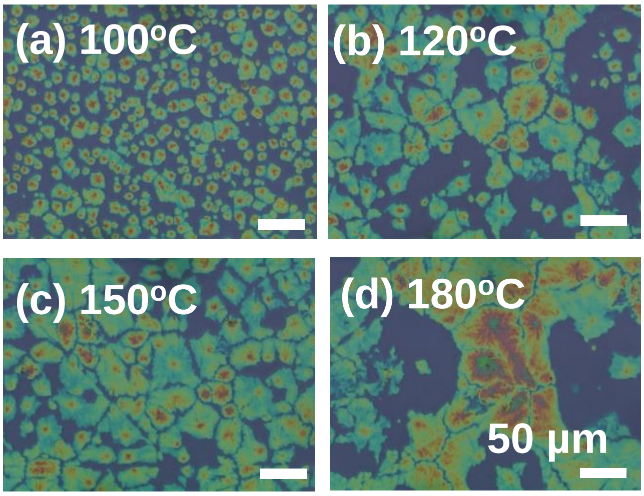

Fig. 3 Photo of organic n-type semiconductor film at variety process temperature. Semiconductor is transferred onto Si/SiO_2 substrate (blue region). Scale bar describes 50 μm.

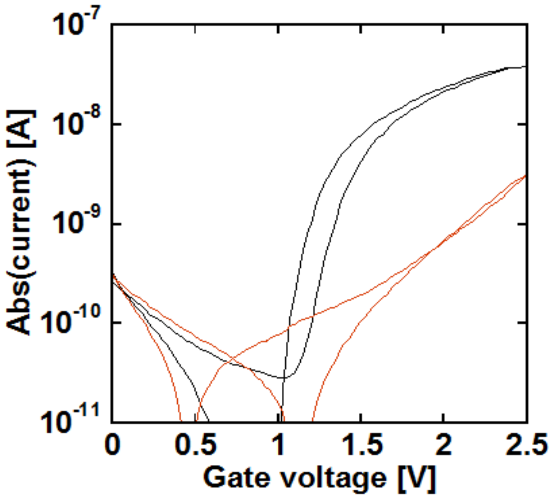

Fig. 4 Transfer curve of TFT with patterned TU-2 film. Black lines show current at drain electrode, and Orange lines shows current at gate electrode through gate insulator.

Si/SiO_2 substrate, as a gate electrode. After that, aluminum layer was exposed to vacuum oxygen plasma for 5 min. to form aluminum oxide layer. Subsequently, we immersed the substrate into isopropyl alcohol solution of self-assembler for 2 hours. In this study, we chose n-octadecyl phosphonic acid as self-assembler. After rinsing solution, we annealed self-assembled monolayer (SAM) at 100 deg.C for 10 min. Then, we formed benzobis(thiadiazole) derivative (TU-2, Ube industries co., Ltd.) thin film onto polydimethylsiloxane (PDMS) by push coating method [7]. 1-methyl naphthalene was chosen as solvent to avoid damage of aluminum layer beneath SAM. We used 0.1wt% solution of TU-2. Revers printing plate with 500 μm square holes was pushed onto TU-2 thin film to make a pattern. We transferred this patterned thin film onto SAM surface (see Fig. 2). Finally, Au was deposited onto the semiconducting layer as source / drain electrodes.

Measurements

To measure transfer characteristics of TFTs, gate voltage is swept from 0 to 2.5 V with drain voltage of 2 V. Mobility is calculated from saturation region of transfer curves. For invertor measurement, we prepare a p-type organic transistor on the other substrate and connect it to TU-2 transistor, electrically, by probes and cables. V_{DD} voltage is set up to 2 V, and we sweep input voltage from 0 to 2 V.

3. Results

Fig. 3 shows thermal dependence of push-coated semiconductor film shapes. Increasing process temperature, semiconductor grain grows more and one domain tends to be larger. Same crystal growth has been reported in p-type polymer conductor, P3HT[7].

Optimized transistor with TU-2 formed directly on SAM shows mobility of 0.06 cm^2/Vs. On the other hand, transistors with patterned TU-2 film drives with mobility of 8×10^4 cm^2/Vs and threshold voltage of -0.1 V. A transfer curve of TFTs with patterned TU-2 is shown in Fig. 4. Complementary inverters also work with 2-V operation voltage and those highest inverter gain is 27 (non-patterned) and 12 (patterned).

4. Conclusions

We have investigated solution process of organic n-type semiconductor. We use push coating method for hydrophobic gate dielectrics. High process temperature makes semiconductor thin film grow larger. TU-2 transistor shows good mobility of 0.06 cm^2/Vs with low operation voltage of 2.5 V. Utilizing reverse offset printing method, we have obtained clear patterns of semiconductor. This patterned TFT also works. Complementary invertor have been fabricated and shown voltage gain of 27 in 2-V operation. Finally, we succeed to obtain high mobility organic n-type TFTs with solution process.

References

[1] Zhang, Fengjiao, et al., *Journal of the American Chemical Society* **135**.6 (2013) 2338-2349.

[2] Soeda, Junshi, et al., *Advanced Materials* **23**.32 (2011) 3681-3685.

[3] Mamada, Masashi, et al., *Chemistry of Materials* **27** (2014) 141-147.

[4] Cheng, Xiaoyang, et al., *Chemistry of materials* **22**.4 (2010) 1559-1566.

[5] Takei, Kuniharu, et al., *Nature materials* **9** (2010) 821-826.

[6] Klauk, Hagen, et al., *Nature* **445** (2007) 745-748.

[7] Ikawa, Mitsuhiro, et al., *Nature commun.* **3** (2012) 1176.