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Integration of High Speed and Low Power CMOS Front-end Circuits with Silicon Photonic Devices

Shawn S. H. Hsu[1], Yan-Feng Li[1], Ching-Hui Liao[1], Po-Chun Wang[1], Yen-Ting Liu[1], Po-Wei Chiu[1], Shen-Wen Chen[1], Ke Li[2], David J. Thomson[2], and Graham T. Reed [2]

[1] Institute of Electronics Engineering, National Tsing Hua University, Hsinchu, Taiwan
858 Delta Bldg., 101, Sec. 2, Kuang-Fu Rd., Hsinchu 30013, Taiwan
Phone: +886-3-5731278, E-mail: shhsu@ee.nthu.edu.tw
[2] Optoelectronics Research Centre, University of Southampton, Southampton, Hampshire, SO17 1BJ, UK

Abstract

In this paper, we present the CMOS front-end circuits for optical transceivers. The design considerations for achieving high speed and low power operation in both transimpedance amplifier (TIA) and modulator driver (MD) are discussed. Also, integration of the CMOS circuits with silicon-based photonic devices such as the Ge-on-Si photo diode and silicon optical modulator is addressed for the high performance silicon-based optical transceiver front-end.

1. Introduction

Booming in the information technology (IT) era changes the way people interacting with each other. This also comes with an urgent need for further advances on high speed data transmission networks. Recently, the concept of fifth generation (5G) communications has been proposed for a significantly increased data rate, where the optical communication plays an essential role in the system architecture [1]. Also, the optical interconnect (OI) has been widely employed in the data centers to link a massive amount of servers. Compared with the wireline communication system based on the electrical interconnects, using the optical approach for data communication promises an increased speed, lowered power consumption, reduced delay, and improved immunity from electromagnetic interference. Fig. 1 illustrates a typical optical communication system. The front-end circuit blocks for OE conversion including the transimpedance amplifier (TIA) and modulator driver (MD) are of extreme importance, which are often a bottleneck to limit the overall system performance. Conventionally, these circuits are realized by the III-V compound semiconductors to take the advantage of superior transistor characteristics. In this study, the CMOS technology is used to realize the front-end circuits for optical transceiver for achieving the goal of high speed and low power operation.

2. Optical Receiver Front-end Circuits

Being the first circuit block in the receiver end, the TIA is critical to determine the overall bandwidth and sensitivity of the system. Different topologies for TIA were proposed to achieve a wide bandwidth under a small power consumption. As shown in Fig. 2(a), the regulated cascode (RGC) topology is widely used to reduce the input resistance, leading to a wide bandwidth. The common-gate (CG) configuration is

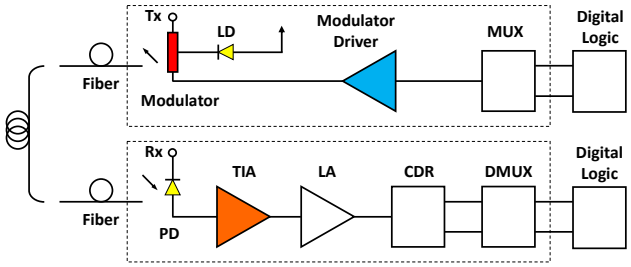

Fig. 1. Typical optical communication system, where the TIA/PD and modulator driver/modulator are very critical for achieving high-speed data transmission.

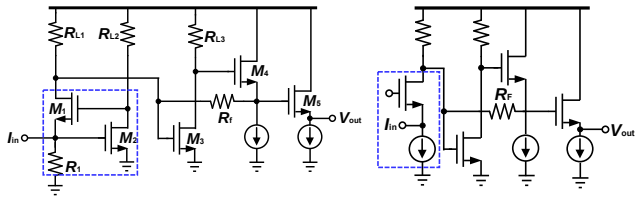

Fig. 2. (a) TIA with the regulated cascode (RGC) input stage (b) TIA with the common-gate (CG) input stage.

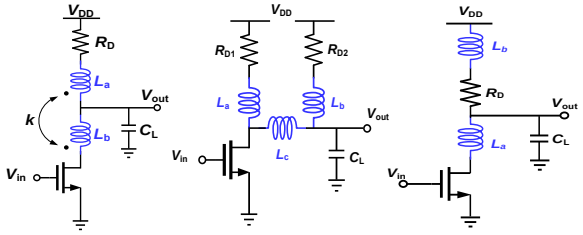

Fig. 3. Different inductive peaking topologies (a) T-coil peaking (b) π-type inductor peaking (c) reversed triple resonance network (RTRN).

also employed for high speed TIA applications, which allows a further reduced bias voltage. Also, the CG-TIA has a decoupled transimpedance gain and input impedance, and can be optimized separately.

One important design technique for the CMOS TIA to achieve a bandwidth up to tens of GHz range is inductive peaking. Different topologies were reported such as the T-coil peaking, π-type inductor peaking [2], and RTRN topology [3]. The bandwidth can be enhanced up 3-5× compared with that without using inductive peaking technique. However, the inductive components often consume a relatively large chip area. Thanks to the technology in advanced CMOS process, the multiple metal layers allow realization

of 3D-type inductor, which can significantly reduce the chip area, while still have much enhanced circuit performance. For example, with a similar inductance, the chip area of 3D inductor can be only 0.07× compared with the conventional 2D spiral inductor in our design for a 20 Gb/s equalizer [4].

3. Optical Transmitter Front-end Circuits

A great challenge of using the advanced CMOS technology for modulator driver design is the relatively small breakdown voltage of the transistor. Although recent advances have reduced the required operating voltage significantly for the silicon modulator to be about 2-4 V (differential, peak-to-peak), this specification is still not easy to be achieved since the typical breakdown voltage for CMOS is only about 1.5-3 V, especially a large bandwidth is also required. The cascode configuration is an effective approach to solve this problem, which stacks two or more of the transistors to enhance the output voltage swing with a reduced voltage across each transistor. Different circuit topologies have been proposed for the modulator driver. The two commonly used designs are the cascade-type topology and distributed amplifier (DA). The former one offers a high voltage gain under low power consumption with a multiplied gain of each stage. On the other hand, the DA provides higher output swing with excellent gain flatness, but relatively large power consumption. Fig. 4(a), 4(b), and 4(c) show our design of CMOS DA for 40 Gb/s applications. Note that each unit gain stage is based on the cascode topology with inductor peaking between the common-source and common-gate stages.

4. Integration with Silicon Photonics Devices

Compared with the III-V-based components for optical communications, the silicon photonic devices offer high quality and low cost solutions with the possibility of a fully-integrated optical transmitter in the silicon platform. The Mach-Zehnder modulator (MZM) on silicon has been reported to achieve an extinction ratio of 10 dB with a bandwidth up to 40 Gb/s and beyond for example [5]. Fig. 5(a) shows the micrograph of the modulator driver in 90-nm CMOS integrated by bond wires with the in-house designed and fabricated silicon modulator. Note the parasitic effects of the bond wires should be considered carefully to prevent the degradation of the OE conversion.

Recent advances have also shown high performance Ge photo detector (PD) on the silicon substrate with excellent sensitivity and large bandwidth. We demonstrate the integrated Ge-on-Si PD with a very low power CMOS TIA, as shown in Fig. 5(b). The TIA is capable of 40 Gb/s operation under power consumption of only 12 mW. It should be mentioned that the circuits could be flip-chip integrated with the silicon photonic devices directly using the silicon substrate as the carrier. With the relatively low cost silicon substrate, this approach allows further increased operating speed without the parasitics introduced by the bond wires. Also, this approach is suitable for the array-type multi-channel system level integration.

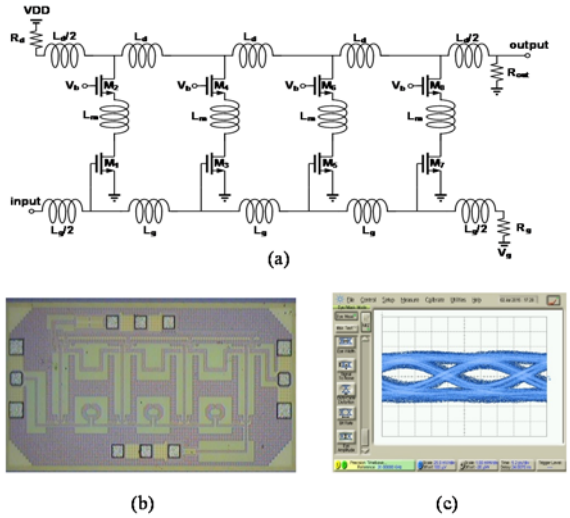

Fig. 4. (a) Proposed circuit topology of distributed amplifier (DA) in 90-nm CMOS (b) chip micrograph (c) measured eye diagram at 40 Gb/s.

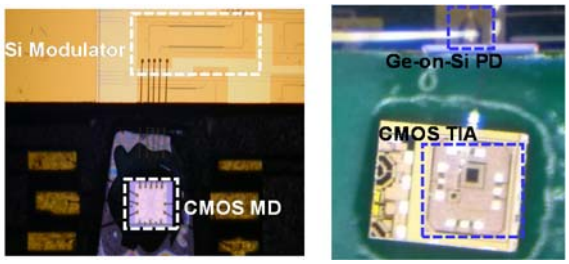

Fig. 5. Wire bond integration of (a) silicon optical modulator with 90-nm CMOS DA. (b) Ge-on-Si PD with 90-nm CMOS TIA.

5. Conclusions

We presented the design of front-end circuit blocks of optical transceiver including the transimpedance amplifier and modulator driver for achieving high speed and low power operation in CMOS technology. The design considerations were discussed and the integration of the CMOS circuits with silicon photonic devices was also addressed.

Acknowledgements

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