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A Wide Dynamic Range CMOS Image Sensor with Two Different Sensitivity Storage Diodes

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Abstract

In this paper, a wide dynamic range (WDR) CMOS image sensor (CIS) is proposed using two different sensitivity storage diodes (SD1 and SD2) implemented by 0.11-μm Dongbu HiTek (DBH) CIS process. A dynamic range (DR) of the proposed imager can be extended by reading signal charges from SD1 and SD2, which are for high- and low-sensitivity, respectively. Ratio of charges in two SDs is determined by supply voltage of shuttle gate (SG). By changing the supply voltage of SG, wide DR of 97dB has been attained.

1. Introduction

Recently, CISs have been greatly improved to increase the operation range of sensor itself from dark to bright scene [1-3]. Some published papers have described the dynamic range (DR) extension ways using 5T pixel [1], multireset algorithm [2], and global multishuttering [3] methods. However, there approaches do not always care about the noise.

In this paper, the novel pixel structure using dual storage diodes (SDs) for wide dynamic range (WDR) has been described and demonstrated with the measurement results. Using two different signals from SDs, a WDR performance can be realized with single frame and the dynamic range is also controlled by a shuttle gate (SG) between pinned photodiode (PPD) and SD2. The dual SDs in a pixel make possible to implement the true-CDS readout operation with the correlated multiple sampling (CMS) technique [4] for the two SDs, which lead to extending the DR for both low- and high-light levels.

2. Operation principle of the proposed imager

Fig. 1 shows a chip layout with proposed WDR pixel structure using two SDs, which are connected to PPD. The SG is located between the PPD and the SD2. The signal electrons, generated in PPD, are accumulated in SD1 and SD2, respectively. The SD1 acts as a storage area for high-sensitivity and the SD2 acts as a storage area for low-sensitivity. Using this difference of signal intensity between the SD1 and the SD2, the DR of proposed CMOS imager can be extended in comparison with the conventional CMOS imagers. By changing potential barrier under SG with different gate voltages (-1V ~ -0.1V), flowing of the electrons is controlled to SD1 and SD2. When the supply voltage for SG is relatively low-level, approximately -1V, most of the signal electrons are transferred to the SD1, only a few of electrons are leaked to the SD2. But the supply voltage for SG is higher, approximately -0.1V, more electrons flow to SD2. The DR is slightly narrowed by changing the SG voltage from -1V to -0.1V, but the SNR is improved at bright scene. One of key point to design is that the excessed signal electrons in SDs should be drained to prevent the flowback to PPD. To do this, a reset transistor (RST) is normally turned on for 1-horizontal (H) cycle except the addressed row of pixels. At the same time, transfer gate (TX) voltage should be optimized to flow the excessed signal charges in SDs to a floating diffusion (FD) node.

3. Experimental results and discussion

Fig. 2 shows the photoelectric conversion characteristics of the proposed imager. As can be seen in Fig. 2 (a), the proposed image sensor has two different photoelectric conversion characteristics (SD1 for high sensitivity and SD2 for low sensitivity). The photo-sensitivity from SD2 is varied by the SG supply voltages. In another word, the SNR of output signal from SD2 can be improved with small DR sacrifice (see Fig. 2 (b)). Using these two output signals from SD1 and SD2, the wide range synthesized output is achieved as shown in Fig. 2 (c). From this result, we can confirm that the maximum DR is 97dB and the prototype WDR imager is successfully worked.

Fig. 3 shows the synthesized image using output signals, which come from SD1 (high-sensitivity) and SD2 (low-sensitivity). In Fig. 3 (a), the image information under the strong illumination condition is loss, because the output signal from SD1 is already saturated. Contrary to this, when the output signal from SD2 is only used, we cannot attain any information from dark scene because of the low-light responsiveness (see Fig. 3 (b)). By synthesizing two images which are readout from SD1 and SD2, the clear image from dark to bright scenes has been reproduced with 97dB DR as can be seen from Fig. 3 (c). As shown in Table I, the noise level the image is very low, indicating that the wide DR is attained by extending it to low- and high-illumination levels.

4. Conclusions

The WDR CIS using SDs is proposed and evaluated. By splitting the signal electrons from PPD to SD1 and SD2 separately, the DR of the proposed CIS is extended. Also, the SNR at the relatively strong light intensity, when SD2 is used,

can be optimized by the SG voltage level. The developed CIS is very suitable for industrial and scientific applications such as the automobile, security, and biomedical imaging.

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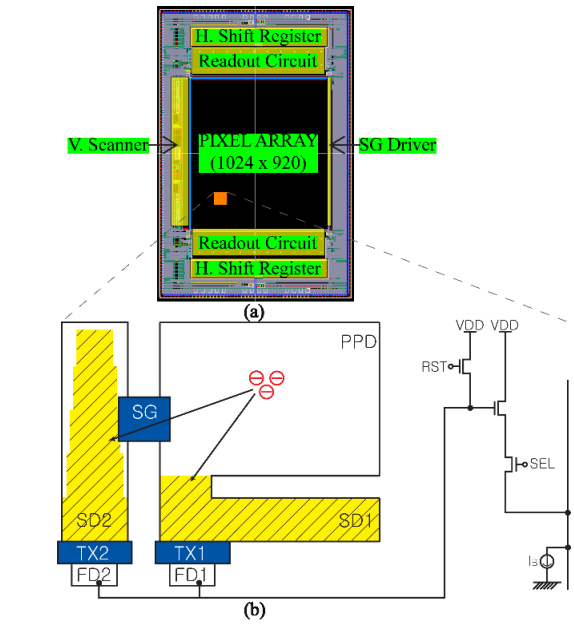
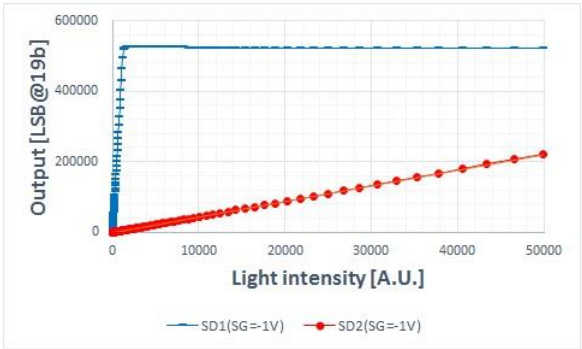
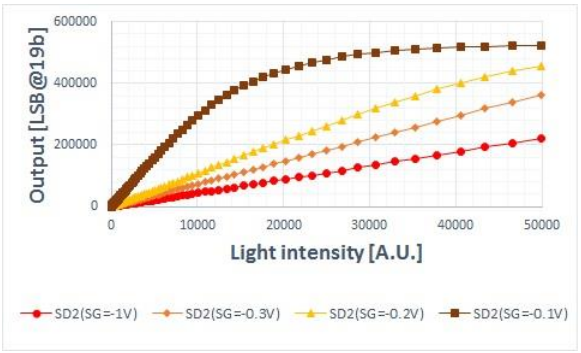


· PPD : Pinned photodiode
· SD : Storage diode
· TX : Transfer gate
· FD : Floating diffusion
· SG : Shuttle gate

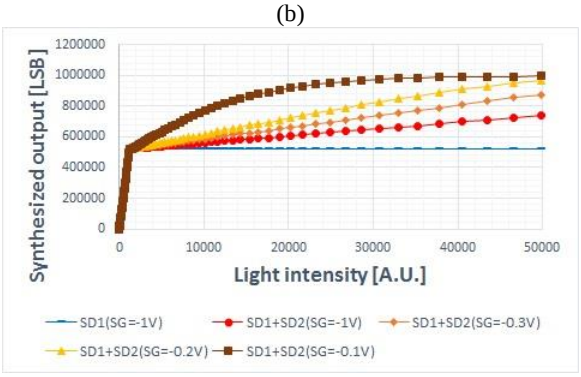
Fig. 1 The proposed WDR CMOS image sensor.
(a) Chip layout. (b) Pixel architecture.



(a)



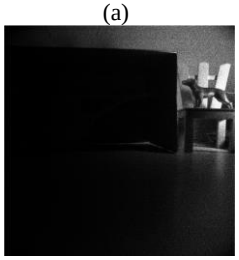
(b)



(c)

Fig. 2 Measured photoelectric conversion characteristics.
(a) Measurement results of SD1 and SD2 (@SG=-1V).
(b) Measurement results of SD2 with different SG voltages.
(c) Synthesized results using SD1 and SD2.

(a)



(b)

(c)

Fig. 3 Captured images.
(a) High sensitivity (SD1).
(b) Low sensitivity (SD2).
(c) Synthesized image (@DR=97dB).

Table I

Chip Characteristic	
Process	0.11-μm Dongbu HiTek CIS
Pixel size	7.1μm x 7.1μm
Pixel Count	1024 (V) x 920 (H)
ADC resolution	19 bit
Conversion Gain [uV/e-]	93.1μV/e-
Noise	1.69e-rms (@peak) 1.80e-rms (@median)
Maximum dynamic Range	97dB (SG=-1V)