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Hurdles and Progress towards Device Applications of Graphene and Layered Materials

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Abstract

Graphene and layered semiconductor materials such as the transition metal dichalcogenides have captured the imagination of scientists and engineers for the last decade with their fascinating electronic and photonic properties. To sustain the initial excitement of discovery, it is now imperative to explore if some of the unique physical features of such materials be turned into useful electronic or photonic devices. Here, I discuss a few such device opportunities, and outline the progress till date, and hurdles ahead.

1. Introduction

The discovery of single-layer graphene in 2004 [1], and the first demonstration of single-layer MoS_2 transistors in 2011 [2] marked intense excitement in the electronic and photonic properties of layered materials. These '2D' materials can be much thinner than their 3D counterparts, and still preserve their electronic and optical integrity down to the last monolayers because of strong in-plane covalent bonds, and weak out of plane van der Waal's bonds. A few device applications that exploit this unique ability of graphene and layered semiconductor materials were thus conceived. Here, I summarize some of our solid-state device proposals, and discuss the progress towards their realization. I identify the key hurdles that need to be overcome, and the ancillary benefits of overcoming these technological hurdles.

2. Graphene Nanoribbon Tunnel-FETs

The tunneling field-effect transistor (TFET) can lower the gate voltage required for turning a transistor from the off to on state below the thermal Boltzmann limit of ~2.303 kT $\ln[I_{on}/I_{off}]$. The lowering of the required voltage for switching will enable energy efficiency of logic circuits. The roadblock for realizing TFETs is the low on-currents possible in conventional semiconductors due to interband tunneling. Very narrow gap semiconductors increase the tunneling current, but also increase the off current. A small choice of narrow-gap 3D semiconductors and heterostructures with staggered or broken gap band alignments offer a potential solution, but upon scaling to nanoscale dimensions, quantum confinement induced increase in the ground state energies, and consequently, an increase in the tunneling gap decreases the on current. Graphene and layered semiconductors offer a potential way around this bottleneck.

Motivated by this argument, in 2008 we proposed to use graphene nanoribbons (GNRs) for realizing tunneling FETs [3]. We evaluated the expected performance of GNR TFETs [4] and benchmarked them against various semiconductors. The key requirements that emerged from this exercise were: GNRs of widths between 5-10 nm with low line-edge roughness, very thin EOTs, controlled doping of high concentrations, and low contact resistances. Each of these challenges required significant advances in the growth, material control, and fabrication. In principle, the GNR TFET is similar to the seminal carbon-nanotube FET [5], but with complete control of the bandgap, doping, and geometries. Based on this theoretical proposal, we launched an experimental effort towards realizing the GNR TFET.

The experimental advances towards the realization of GNR TFETs has been slow, but steady. Initial demonstration of thin GNR channel FETs indicated the presence of bandgaps [6] and high current carrying capacity [7], but the lack of a chemical doping strategy only enabled Schottky-type contacts with low room-temperature modulation [8, 9, 10, 11]. Chemical doping still remains a challenge. GNR array FETs starting from single-layer graphene on SiC with top gates have been realized, exhibiting high current drives. The major singular challenge at this stage is the controlled chemical doping of the GNRs. Unlike carbon nanotubes, the broken bonds of a GNR allow for chemical substitutional doping, but no clear strategy has been identified till date for controllable and stable doping. The challenge of ohmic contacts is tied to the challenge of doping, and a breakthrough in this area is needed to take GNR FETs and GNR TFETs to the next logical step. GNR FETs are themselves highly attractive for extending CMOS scaling, and can be considered a high-value ancillary benefit in the drive towards realizing the GNR TFET.

3. SymFETs and Interlayer Tunnel-FETs

In 2012, motivated by the question of the single-particle counterpart of the novel proposal for graphene-based BisFET [12], the question of interlayer tunneling between 2D graphene layers was investigated by Feenstra, Gu, and me [13]. From the theoretical evaluation, we predicted that a strong negative differential resistance robust to temperature should occur because of interlayer tunneling dictated by the density of states overlap. That this transport mechanism occurs be-

tween atomically thin 2D layered materials makes it electrostatically gateable to very high level of degeneracies, and voltage-controlled high-frequency oscillations. Based on these observations, we proposed the concept of a SymFET [14]. This device was experimentally realized by the groups in Nottingham led by Eaves and at Manchester led by Novoselov/Geim [15], and oscillations were observed soon thereafter by that group [16]. The SymFET is a device that does not require the opening of a bandgap, and potentially could have applications in high-frequency RF applications.

That the interlayer graphene SymFET does not have a large current modulation makes it unattractive for Boolean logic switching. However, around the same time as such graphene devices were being investigated, the first reports of single-layer MoS_2 FETs from Kis's group in EPFL were presented [2], showing monolayer semiconductors with well-defined bandgaps unlike graphene. Such monolayer and multilayer semiconductor FETs could potentially be converted into interlayer tunneling FETs that will exhibit NDR and very large on-off ratios, with sharpness well below the Boltzmann limit. The gapped layered semiconductors thus offered an obvious solution to the modulation problem [17, 18]. Because of the relatively large bandgaps of transition metal dichalcogenide (TMD) semiconductors, the interband tunneling currents in planar p-n Esaki diodes would not be very high [19], but by taking advantage of interlayer tunneling with staggered and broken gap band alignments, one could potentially make a very high performance TFET [20]. An embodiment of this idea, called the ThinTFET for *t*wo-dimensional *h*eterostructure *in*terlayer *TFET* was thus proposed [21]. This class of devices borrow the best ideas of III-V TFETs and merge them with the advantages of layered 2D crystal semiconductor heterostructures. The challenges in realizing it are high, but significant ancillary benefits can be expected in the path of overcoming them, such as ultrascaled FETs [22].

Interlayer tunneling between TMD layers such as MoS_2/WSe_2 and monolayer $MoSe_2/WSe_2$, and even in broken gap layered mismatched heterostructures such as black phosphorus/$SnSe_2$ were observed, the latter exhibiting strong room temperature NDR behavior, and low temperature dependence of interband tunneling currents [23, 24, 25]. Photocurrent spectroscopy measurements indicate that some of these heterostructures (such as black phosphorus/$SnSe_2$) have a broken-gap band alignment, which is very well suited for high performance TFETs. Based on such TMD layers, very recently the first demonstrations of interlayer TFETs have been reported [26] with ionic-gating, and more are currently being presented at workshops and conferences, and should be published soon.

Several promises and challenges of the 2D crystal approach to making solid-state transistors – both traditional, and 'novel', are outlined in the review article [27]. In spite of rapid progress in the above device demonstrations, they remain highly dependent on the laboratory where the measurements were performed. Many use exfoliated flakes with layer transfer, sometimes combined with demonstration vehicles such as ionic liquid gating or other forms of "electrostatic doping" which typically is a decent vehicle for the demonstration of a concept if performed in a controlled manner. But the two major hurdles that stand today between the first crude demonstration phases, and unleashing the true potential of these layered materials are a) the inability to epitaxially grow low-defect layers and heterostructures, and b) the inability to substitutional dope the layers with donors and acceptors.

4. Conclusions

The first generation of electronic devices based on graphene and layered materials have shown promise for RF and low-power digital logic switching. However, significant challenges in the epitaxial growth and doping of these materials must be overcome at this stage to make progress towards realistic applications.

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Appendix

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