Extended Abstracts of the 2016 International Conference on Solid State Devices and Materials, Tsukuba, 2016, pp435-436

J-3-01(Invited)

Carbon Nanotube Transistor Technology for Scaling Beyond Si CMOS

Qing Cao[1]

[1] IBM T.J. Watson Research Center
1101 Kitchawan Rd., Yorktown Heights, NY 10598, USA
Phone: +1-914-945-4904 E-mail: qcao@us.ibm.com

Abstract

Carbon nanotubes are a promising candidate to replace silicon as the semiconductor channel in extremely-scaled high-performance field-effect transistors with their exceptional electrical properties. However, there are several daunting challenges to overcome for nanotube transistors to become a serious device technology competing with Si and III-V. Here we introduce our latest progress on addressing these device and material issues, and demonstrate the feasibility of building high-performance logic devices at 5 nm technology node and beyond based on single-walled carbon nanotubes.

1. Introduction

Conventional scaling of Si complementary metal-oxide semiconductor (CMOS) devices provided ever-improved transistor performance, density, power, and cost in the last four decades. However, it has become very difficult in recent 10 years with Si devices approaching their physical limits. In search for the next switch beyond silicon, carbon nanotubes are a very promising candidate, with a saturation velocity several times faster than silicon and intrinsic thinness (~ 1 nm in diameter) which enables superior electrostatic control to minimize the off-state leakage current even at ultra-small device dimensions. Here we discuss our recent advances in building high-performance nanotube transistors with extremely scaled device dimensions including both device channel length (L_{ch}) and contact length (L_c), separation of nanotubes based on their electronic types, and assembly techniques for forming nanotube arrays with high semiconducting nanotube purity and tight pitch. These results suggest that replacing Si with carbon nanotubes in high-performance logic devices at 5 nm technology node and beyond is feasible.

2. The Scalability of Carbon Nanotube Transistors

At 5 nm technology node, both L_{ch} and L_c need to be scaled down to sub-10 nm regime. In experiment, we find that nanotube transistor still demonstrated exceptional device performance with its L_{ch} scaled down to sub-10 nm as shown in Figure 1 [1]. With their intrinsic ultrathin body, these devices exhibit excellent short channel control, with device subthreshold swing as small as around 90 mV/dec. In the meantime, with their unique confined quasi-one-dimensional structure, carbon nanotubes have high optical phonon energy, and thus a saturation velocity (v_{sat}) about five times higher than that of silicon. Such high v_{sat} allows these nanotube transistors to deliver the highest current density compared to previously reported sub10-nm L_{ch} devices based any semiconductor materials or any device structure.

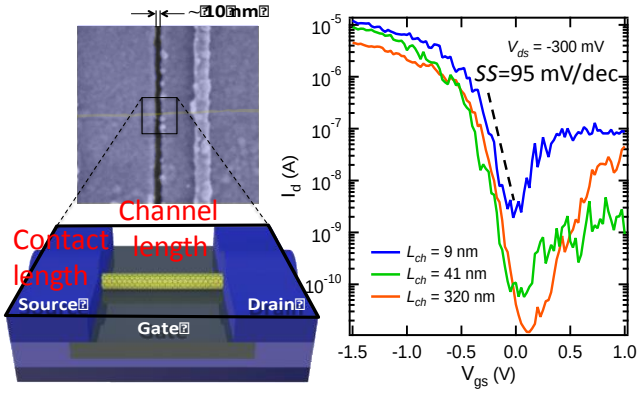

Fig. 1 Schematic, false-colored SEM image, and transfer characteristics of nanotube transistor with L_{ch} down to 9 nm.

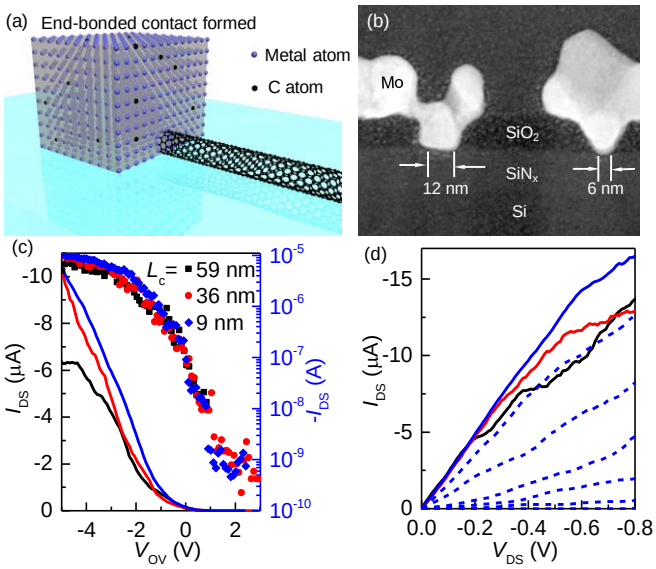

Fig. 2 Schematic (a), cross-sectional TEM image (b), transfer (c) and IV (d) characteristics of nanotube transistor with L_c down to 9 nm.

For scaling, device L_c need to be reduced to 10 nm as well. However, for conventional side-bonded contacts to nanotubes, where metals are deposited on top of the nanotube and couple with the nanotube through weak van der Waals interaction, the parasitic contacts resistance ($2R_c$) increases reciprocally with the reduction of L_c, leading to very high $2R_c$. One way to solve this limitation is to convert the contact structure into

end-bonded contacts, where metals are coupled with the opened ends of nanotubes through strongly coupled covalent bonds. In this structure, all carriers from the nanotube channel will be either collected into the metal contacts or get reflected back right at this quasi-zero-dimensional interface, and thus the $2R_c$ will be independent of L_c. We realized this end-bonded contact structure utilizing the solid state chemical reaction between nanotube and deposited Molybdenum [2]. The formed p-type end-bonded contacts demonstrate zero Schottky barrier, and a size independent $2R_c$ down to ~30 kΩ per tube even with L_c below 10 nm, as illustrated in Figure 2.

These results demonstrate that it is possible for nanotube transistors to deliver exceptional device performance with device dimensions scaled for 5 nm node, a capability that has not been successfully demonstrated in other materials.

3. Overcoming Manufacturability Challenges for Nanotube Transistors

Several manufacturability issues have to be solved for carbon nanotube transistors become a serious device technology. First of all, nanotubes must be sorted based on their electronic types to very high purity so that we could build devices based on only semiconducting nanotubes. We developed a sorting technique based on the selective redox reaction between nanotubes and oxygen dissolved in water [3]. By carefully tuning the pH, the energy levels of oxygen can be precisely tuned so that they only dope metallic nanotubes, as illustrated in Figure 3. These reacted metallic nanotubes demonstrate positive surface charge and then can be easily sorted out using high throughput chromatography method. The semiconducting nanotubes can then be enriched to a purity above 99.94% as verified by direct electrical measurements (Figure 3c).

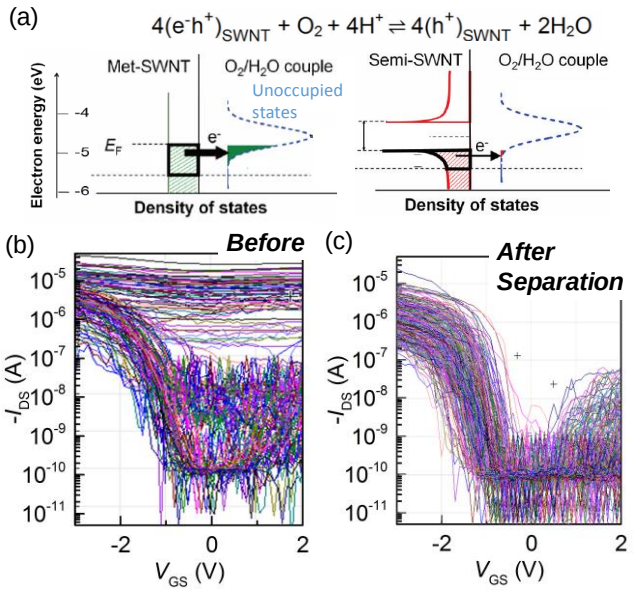

Fig. 3 Schematic (a) showing the mechanism for the separation of nanotubes based on their electronic types using redox reaction. Collection of transfer curves measured for devices made using nanotube solutions before (b) and after (c) sorting.

These sorted nanotubes can then be assembled into well aligned arrays suitable for adoption in high performance transistors [4]. Langmuir Schaefer method can create arrays of semiconducting nanotubes with almost perfect alignment, self-limited space between neighboring nanotubes down to around 0.5 nm, and thus enormous tube density above 500 tubes per micron as shown in Figure 4 [5]. Here pre-sorted high purity semiconducting nanotubes are first dispersed on a water surface. These floating nanotubes spread out to cover the water surface thanks to surface tension. A compressive force is then applied to assemble nanotubes confined at this two dimensional air-water interface into well-order arrays. The compression stops only after the nanotube arrays cover the whole surface and the film becomes incompressible. The resulted nanotube arrays exhibit unprecedented high nanotube density. This nanotube density leads to record-high current density in active nanotube transistors, and make them become a serious competitor with silicon in high performance metal-oxide-semiconductor field-effect transistors.

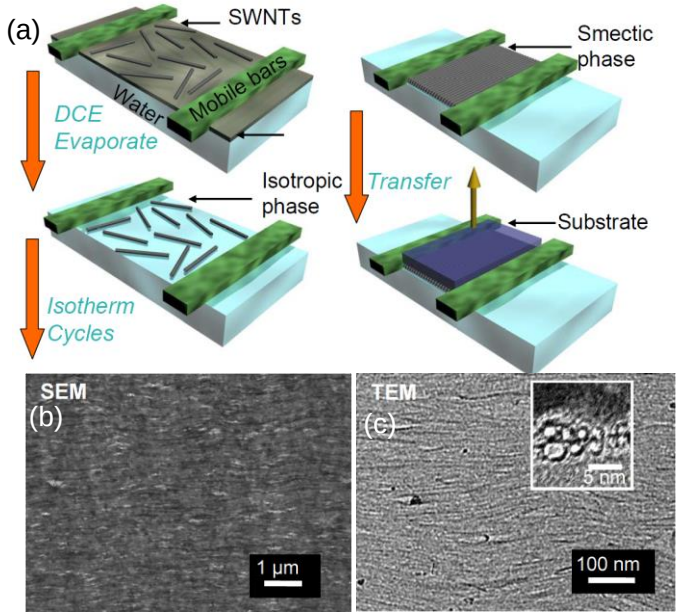

Fig. 4 Schematic (a), SEM (b), and TEM (c) images of nanotube arrays assembled using the Langmuir-Schaefer method.

4. Conclusions

Our recent progress suggests that it is a promising direction to develop the ultimately-scaled transistors based on carbon nanotubes [6].

References

[1] A. D. Franklin, M. Luisier, S.-J. Han, G. Tulevski, C. M. Breslin, L. Gignac, M. S. Lundstrom, and W. Haensch, Nano Lett. **12** (2012) 758.
[2] Q. Cao, S.-J. Han, J. Tersoff, A. D. Franklin, Y. Zhu, Z. Zhang, G. S. Tulevski, J. Tang, and W. Haensch, Science **350** (2015) 68.
[3] J. Wang, T. D. Nguyen, Q. Cao, Y. Wang, M. Y. C. Tan, and M. B. Chan-Park, ACS Nano **10** (2016) 3222.
[4] Q. Cao, S.-j. Han, and G. S. Tulevski, Nat. Commun. **5** (2014) 5071.
[5] Q. Cao, S.-j. Han, G. S. Tulevski, Y. Zhu, D. D. Lu, and W. Haensch, Nat. Nanotechnol. **8** (2013) 180.
[6] Q. Cao, and S.-J. Han, Nanoscale **5** (2013) 8852.