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Voltage Tolerant Circuit Design for Fully CMOS Compatible Differential MTP Non-Volatile Memories

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Abstract

This abstract proposes a fully CMOS compatible differential multiple-time programmable (DFMTP) non-volatile memory (NVM) circuits using the standard TSMC 0.18 μm CMOS process without violating the design/electrical rules. The special voltage tolerant circuits include the bit line (BL) and control gate (CG) drivers for -3V and 6V program/erase operations, as well as the negative voltage isolation circuits for sense amplifiers. The small memory array with these voltage tolerant control circuits was implemented to confirm the correct program/erase/read operations.

1. Introduction

The differential multiple-time programmable (DFMTP) NVM has been proposed using the standard CMOS logic process without extra process steps [1, 2]. However, both of them employ Fowler–Nordheim tunneling (FNT) to erase or/and program data. FNT usually requires more than 10V for operation, which needs complicated peripheral circuits. The new operation of the MTP NVM was proposed using 7nm gate-oxide 3.3V I/O devices [3] biased at 6V and -3V for program and erase in the 0.18μm CMOS logic process. To allow those special biases working in the standard CMOS processes, the DFMTP array with voltage tolerant circuits were designed and verified by measurement.

2. The DFMTP Cell and System Architecture

The DFMTP cell shown in Fig. 1 similar to the one in Ref. [3] is composed of three 3.3V PMOS transistors and two control-gate coupling PMOS transistors (CG0 and CG1). The word line (WL) or SG is used to pass the source line (SL) voltage to the sources of floating gate transistors (FG0 and FG1). The advantage of the differential structure is easier to distinguish the small current difference between FG0 and FG1 Transistors. Since hot-hole injection and hot-electron injection are used for program and erase, respectively, the bias voltages can be reduced. Table I lists the bias conditions of program, erase and read operations.

In Table I, we can observe that the BL0 and BL1 nodes could be biased to floating, -3V or 0V. The corresponding BL drivers are required. The sense amplifiers (SA) needs to be disconnected to the BL0 and BL1 during program/erase, so the negative voltage isolation circuits are placed between the BL driver and the SA. Besides, the CG0/CG1 nodes may be biased at 6V which is higher than the standard 3.3V during program/erase, so the voltage tolerable CG drivers are required.

Fig. 2 illustrates the architecture of the test die to control the DFMTP memory array with 4 WLs with A0 and A1 as the address bits, as well as four bits per WL. din, dout and vrpout are the inputs, outputs and verified signals, respectively. If the cells are programmed to the correct data, vrpout will be low. To select the correct WL bias, the WL drivers with voltage select are acted as the interfaces between the address decoder and the DFMTP memory array. The CG and BL drivers provide the corresponding biases for CGs and BLs. The negative voltage isolation circuit is placed between the BL driver and the SA. The verifying circuit is used to report whether the memory cells are programmed or erased successfully.

3. Voltage Tolerant Circuits

The circuit blocks marked by the bold lines in Fig. 2 are the voltage tolerant circuits. Fig. 3 shows the CG driver with the table of control signals to produce the desired CG voltage. The supply voltages VDD6 and VDD3 are 6V and 3V, respectively. For instance, during program or erase 1, cgc become 0V, and 6V is passed to CG. Mod5 and Mod6 are off owing to their V_{gs} = 0, while $|V_{ds}|$ of them are 3V. Fig. 4 shows the BL driver with the table of control signals to produce the desired BL0/BL1. The supply voltage is 3V and V_{SS} = –3V. During program or erase 0, the blue cross marks indicate the “off” transistors and the red dotted lines show the signal paths to BL0 and BL1. Note that the voltage drops between any two terminals of all transistors are always within 3V in the CG/BL drivers.

The current sense amplifier (SA) sinks the current from the BL0 and BL1 to the nodes sainl and sainr as shown in Fig. 5 with the table of bias conditions of the negative voltage isolation. Owing to the differential BL0 and BL1, small current difference between them can be sensed. When BL0 or BL1 is -3V during program or erase, LH2 = ROS2 = -3V with sainl and sainr are reset to 0. Thus, no nodes in the SA encounter negative voltages.

4. Implementation and Measurement Results

The test die was implemented using the TSMC 0.18 μm CMOS process. The die microphotograph with core area of 253μm×378μm is shown in Fig. 6. The circuit blocks are numbered from 1 to 6 in the following orders, address buffers/decoders plus WL drivers with voltage select, CG drivers, BL drivers, the small MTP memory array, SAs with negative voltage isolation circuits/data verifying circuits/output buffers, and data input buffers.

After the data are programmed in the DFMTP memory cells, two different WL lines are activated alternatively to read data 0 and 1 repeatedly. Fig. 7 demonstrates the measured waveforms of two outputs (Daout3, Daout4) out of

four. When “enable” drops to 0, the data are sensed to the outputs. The verifying signal Vrpout3 is not utilized in read operation.

5. Conclusions

Voltage tolerant circuits for DFMTP memories using the TSMC 0.18 μm CMOS technology were proposed and verified by measurement. Both the DFMTP memory cells and the circuits were designed without design rules violation and extra process steps. The measurement results reveal the correct program/erase capabilities within 1 ms, and the time to random read is within 15 ns.

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References

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Table I Bias conditions of the DFMTP cell

	BL0 (V)	BL1 (V)	WL (SG) select	WL (SG) un-select	SL= N-Well	CG0= CG1
Prog. 0	-3	0	0 V	3 V	3.3 V	0 V
Prog. 1	0	-3	0 V	3 V	3.3 V	6 V
Erase 0	-3	0	0 V	3 V	3.3 V	0 V
Erase 1	0	-3	0 V	3 V	3.3 V	6 V
Read	float	float	<1.8 V	3 V	3 V	0.5 V

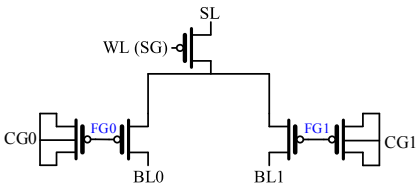


Fig. 1 One DFMTP cell

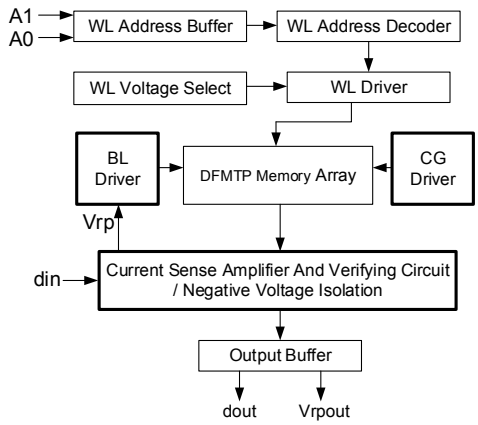
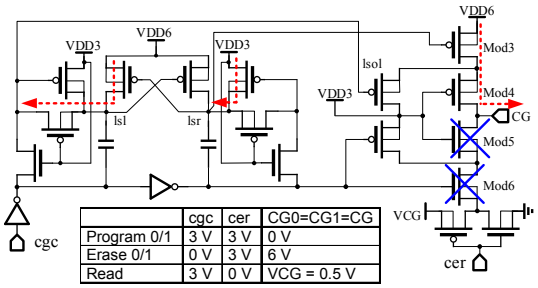


Fig. 2 The circuit architecture of DFMTP memory



	cgc	cer	CG0=CG1=CG
Program 0/1	3 V	3 V	0 V
Erase 0/1	0 V	3 V	6 V
Read	3 V	0 V	VCG = 0.5 V

Fig. 3 Conduction of CG driver when the output CG is VDD6 = 6V.

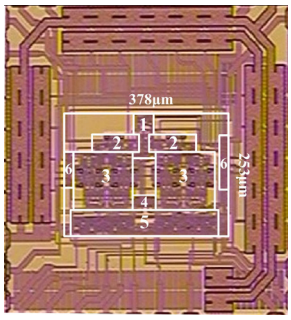


Fig. 6 The die microphotograph

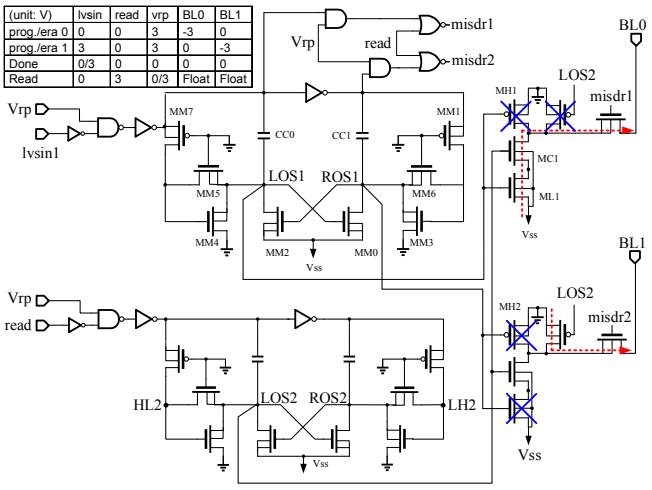
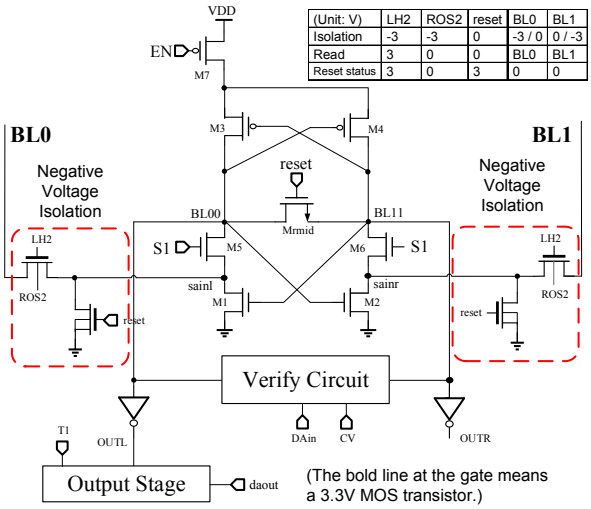


Fig. 4 Conduction of BL driver when BL0 = V_{SS} = -3V, BL1 = 0V.



(Unit: V)	LH2	ROS2	reset	BL0	BL1
Isolation	-3	-3	0	-3 / 0	0 / -3
Read	3	0	0	BL0	BL1
Reset status	3	0	3	0	0

Fig. 5 The SA with negative voltage isolation

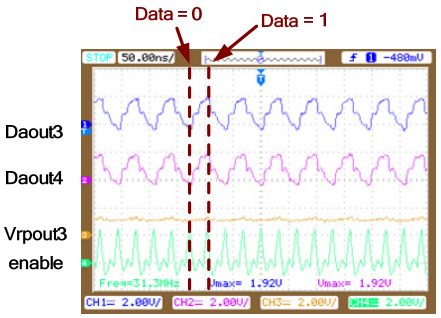


Fig. 7 Waveforms of data outputs from two different addresses read alternatively when the DFMTP memory cells are programmed to 0 and 1, respectively.