

A Wearable Biomedical Sensing System with Normally-off Computing Architecture and Physical Activity Classification Algorithm

Masahiko Yoshimoto¹

¹ Department of Information Science, Graduate School of System Informatics, Kobe Univ.
1-1, Rokkodai, Nada, Kobe, Hyogo 657-8501, JAPAN
Phone: +81-78-803-6630
E-mail: yosimoto@cs.kobe-u.ac.jp

Abstract

This paper describes a wearable bio-medical sensing system, which features monitorings of heart-rate and tri-axial acceleration using a newly developed SoC. A Non-volatile MCU(NVMCU) based on FeRAM for normally-off computing and a noise-tolerant IHR detector have been employed for the SoC design. The SoC consumes 6.14uA for heart-rate monitoring. The sensing system consumes totally ~ 20uA, allowing two-weeks continuous sensing only using a 10-mAh thin-type lithium-ion battery.

1. Introduction

It is well known that the aging problem is getting more serious worldwide. To solve the problem, daily-life monitoring is especially important in preventing lifestyle diseases. Our goal is the monitoring of vital signals and physical activity in daily life to improve users' quality of life.

This report describes a wearable biosignal monitoring system, which can acquire long-term instantaneous heart rate (IHR) data and an acceleration value. The IHR is calculated from the interval of R-waves in electrocardiogram (ECG). The physical activities in daily life (e.g., locomotive, household activities) are classifiable using a triaxial acceleration and IHR.

To enhance the wearable system usability, battery mass and power consumption must be reduced. However, strict limitations on power consumption and electrode distance of wearable ECG monitors makes devices sensitive to various kinds of noises. Especially, if a subject is not at rest (e.g. during exercise), the signal-to-noise ratio (SNR) of ECG signals will be significantly degraded. To realize the low-power and noise-tolerant system, we proposed the SoC using normally-off architecture[1][2] and robust IHR monitor[3].

2. System Description

Figure 1 presents an overview of the wearable healthcare system, comprising the proposed SoC, Near Field Communication (NFC) tag IC, and accelerometer IC. The NFC is used for program loading, individual optimization, and data retrieval from the SoC.

A normally-off computing architecture has been introduced to achieve low power characteristics. The proposed SoC consists of an ECG sensing block, NVMCU, and extra interfaces (see Fig. 2)[2]. The ECG sensing block has an analog front end (AFE), an 8-bit SAR ADC, and a robust IHR

extractor. The NVMCU includes a Cortex M0 (CM0) core with ferroelectric-based non-volatile FFs (NVFF) [1], a 16Kbyte 6T-4C NVRAM for instruction and data memory, and peripherals.

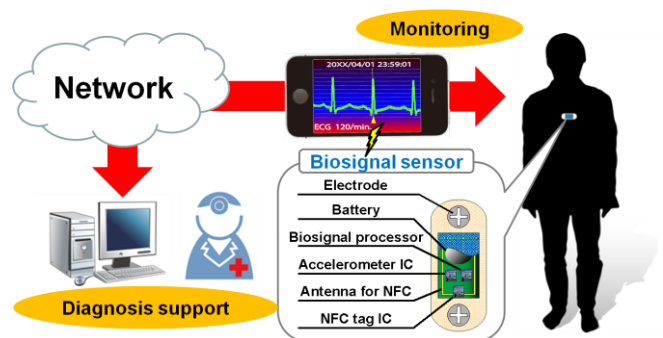


Fig. 1 Overview of the wearable healthcare system

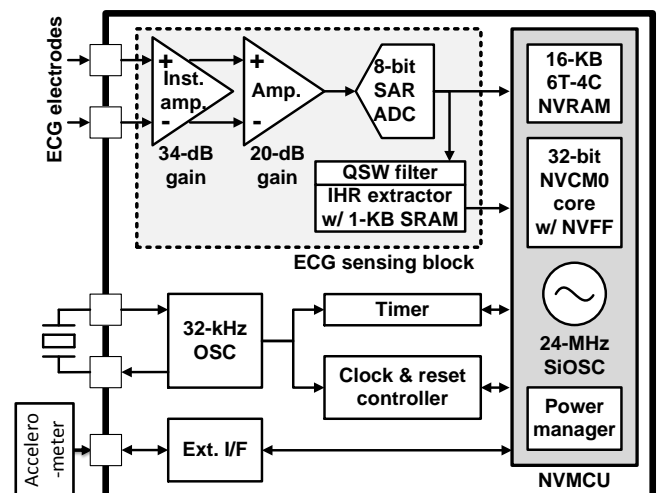


Fig. 2 SoC block diagram for biomedical sensor[2]

3. Normally-off computing architecture

Figure 3 summarizes frequency component of several biosignals. Because the frequency range of biosignals is low, both the standby power reduction and sleep time maximization is efficient for system level power reduction. The normally-off computing technique has been adopted to the buffer memory. The technique is the method to turn off when it is not in use. The blue line shows power consumption transition in case of volatile memory and the red one shows that in case of non-volatile memory in Fig.3.

	Frequency component
ECG	0.01 - 250Hz
EEG	0 - 150Hz
ECoG	0 - 150Hz
EMG	0 - 10 kHz

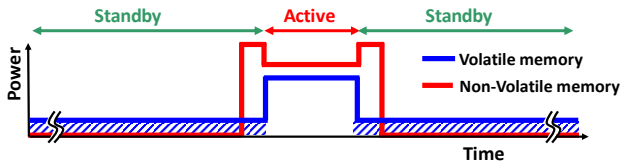


Fig. 3 Frequency component of several biosignals and power transition in case of normally-off computing.

The non-volatile memory drastically reduces the leakage current because the power supply can be gated in the standby mode. We utilized FeRAM as a non-volatile memory. A 6T-4C memory cell which couples SRAM-cell and Ferroelectric capacitor has been developed to realize both non-volatility and fast access characteristics. The non-volatile technique was also introduced into all of F/F embedded in the NVMCU[4]. It minimizes transition overheads, allowing a standby period maximization.

4. Physical Activity Group Classification Algorithm

A physical activity classification algorithm[5] is proposed for energy expenditure estimation. The proposed algorithm can improve the classification accuracy using both the triaxial acceleration and heart rate. It employs three indices: the heart rate reserve (%HRreserve), the filtered triaxial acceleration, and the ratio of filtered and unfiltered acceleration. The percentage HRreserve is calculated using the heart rate at rest condition and the maximum heart rate, which is calculated using Karvonen Formula. Using these three indices, a decision tree is constructed to classify physical activities into five classes: sedentary, household, moderate (excluding locomotive), locomotive, and vigorous. The Algorithm was realized on MCU embedded in the SoC.

5. Fabrication and evaluation results

The 3.7x4.3 mm² test chip has been fabricated using 0.13-um CMOS technology. Fig. 4 shows the chip photomicrograph and characteristics summary. The operating voltage is 1.2 V for AFE, ADC, 24-MHz oscillator, IHR extractor, NVMCU, and other digital blocks. Only the 32-kHz oscillator and IO circuits are operated with 3.0-V supply voltage. The current consumption is 6.14 uA on average with IHR logging application, including 1.28-uA non-volatile MCU and 0.7-uA heart rate extractor. The system containing the SoC, accelerometer IC and NFC tag IC, consumes totally ~20uA.

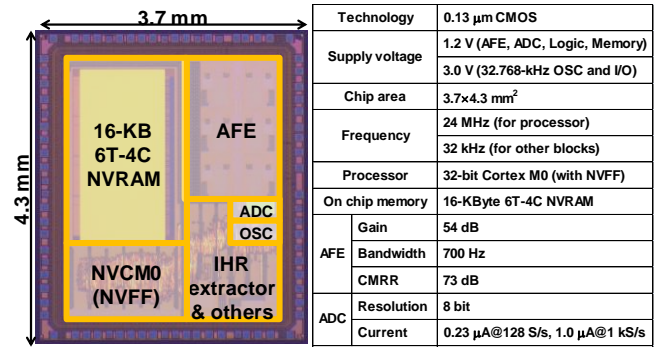


Fig. 4 Photomicrograph and characteristics of SoC

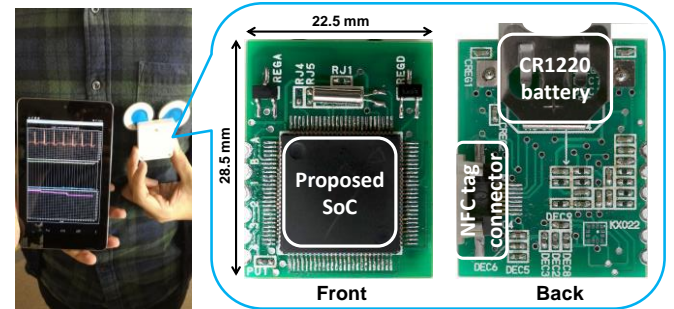


Fig. 5 Photo of experimental biomedical sensor module

6. Conclusions

A wearable biomedical sensing system integrating the newly designed SoC has been developed. Its low power feature was realized by normally-off computing architecture based on non-volatile FeRAM. It consumes totally ~20uA. It realizes two-weeks continuous sensing only using a 10-mAh thin-type lithium-ion battery.

References

- [1] S. Izumi, K. Yamashita, M. Nakano, H. Kawaguchi, H. Kimura, K. Marumoto, T. Fuchikami, Y. Fujimori, H. Nakajima, T. Shiga, and M. Yoshimoto, "A Wearable Healthcare System with a 13.7 μ A Noise Tolerant ECG Processor," *IEEE Trans. BioCAS*, Nov. 2014. (to be published, DOI: 10.1109/TBCAS.2014.2362307)
- [2] S. Izumi, K. Yamashita, M. Nakano, S. Yoshimoto, T. Nakagawa, Y. Nakai, H. Kawaguchi, H. Kimura, K. Marumoto, T. Fuchikami, Y. Fujimori, H. Nakajima, T. Shiga, and M. Yoshimoto, "Normally Off ECG SoC With Non-Volatile MCU and Noise Tolerant Heartbeat Detector," *IEEE Transactions on Biomedical Circuits and Systems*, vol.9, no.5, pp.641-651, Oct. 2015. doi: 10.1109/TBCAS.2015.2452906
- [3] M. Nakano, T. Konishi, S. Izumi, H. Kawaguchi, and M. Yoshimoto, "Instantaneous Heart Rate detection using short-time autocorrelation for wearable healthcare systems," *Proc. of IEEE EMBC*, pp. 6703-6706, Aug. 2012.
- [4] H. Kimura, T. Fuchikami, K. Marumoto, Y. Fujimori, S. Izumi, H. Kawaguchi, and M. Yoshimoto, "A 2.4 pJ Ferroelectric-Based Non-Volatile Flip-Flop with 10-Year Data Retention Capability," *Proceedings of IEEE Asian Solid-State Circuits Conference (A-SSCC)*, pp. 21-24, Nov. 2014.
- [5] M. Nakanishi *et al.*, "Physical activity group classification algorithm using triaxial acceleration and heart rate," *Conference Proceedings: Annual International Conference of the IEEE EMBS 2015*, Milano, pp. 510-513, 2015