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A Self-Biased Low-Dropout Linear Regulator for Ultra-low Power Battery Management

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Abstract

This paper presents a self-biased low-dropout linear regulator (SB-LDO) for ultra-low power battery management. The SB-LDO employs a current feedback circuit to achieve highly accurate and efficient operation. Measurement results demonstrated that the proposed SB-LDO operates with ultra-low quiescent current of 151 nA. The maximum output current was 1 mA, when the input and output voltage were 4.25 and 4.16 V, respectively.

1. Introduction

Energy storage devices are an indispensable component for next generation power-aware small-sized energy harvesting applications [1]. A thin film Li-ion secondary battery is a good candidate for storing harvested energy [2]. However, because a Li-ion battery must be protected from overcharge voltage (e.g., typical charging voltage is 4.2 V), the charging voltage must be carefully regulated. Figure 1 shows a block diagram of the battery charger. Low-dropout regulators (LDOs) are commonly used for battery charging applications to protect a battery against overvoltage [3, 4]. However, because the conventional LDOs dissipate large quiescent currents, we have to design an LDO as low power as possible. Therefore, a highly accurate and efficient LDO is strongly required for ultra-low power Li-ion battery management.

In this paper, we propose a self-biased (SB) LDO employing a current feedback technique to achieve highly accurate, ultra-low quiescent current, and highly efficient voltage regulation. Details of the circuit are as follows.

2. Architecture and circuit design

Figure 2 shows a simplified schematic of the proposed SB-LDO. It consists of a differential amplifier (DA), current feedback circuit (CFC), and output stage. Note that, in our SB-LDO, a current reference circuit to bias the DA is not used. When output current I_{OUT} changes, bias currents in the LDO adaptively change to maintain $V_{FB} = V_{REF}$, where V_{FB} and V_{REF} are the feedback and reference voltages. The circuit achieves high accuracy and ultra-low quiescent current by using a feedback loop with CFC. Details of the operation are as follows.

The current mirror gains of the nMOS (MN2:MP3) and pMOS (MP3:MP4:MP5) transistors are set to 1:2 and 1:1:α, respectively. When I_{OUT} becomes large, the output voltage V_{OUT} and the feedback voltage V_{FB} decrease. Then, I_2, I_3, and I_{OUT} increase. Therefore, V_{OUT} and V_{FB} increase to maintain $V_{FB} = V_{REF}$.

In a steady state, I_1, I_2, and I_3 settle to $2I_1 = 2I_2 = I_3 = (I_{OUT} + I_{FB})/\alpha$, where I_{FB} is the current flowing in the feedback resistors R_1 and R_2. The current use efficiency of the proposed SB-LDO can be defined as

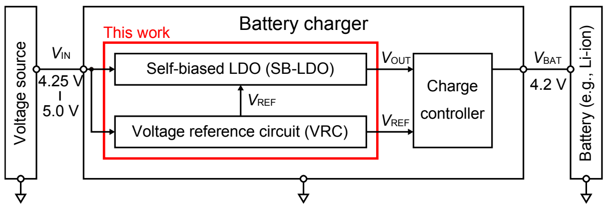

Fig. 1 Battery charger.

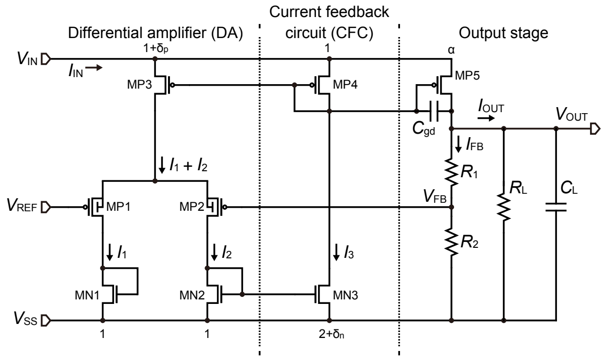

Fig. 2 Schematic of proposed LDO.

$$\frac{I_{OUT}}{I_{IN}} = \frac{I_{OUT}}{I_1 + I_2 + I_3 + I_{OUT} + I_{FB}} = \frac{\alpha}{\alpha + 2} \cdot \frac{I_{OUT}}{I_{OUT} + I_{FB}}. \qquad (1)$$

Therefore, the larger the α, the higher the efficiency.

In the sub-threshold region of MOSFETs, I_2 can be expressed as

$$I_2 = \frac{I_1 + I_2}{1 + \exp\{(V_{REF} - V_{FB})/(nV_T)\}}, \qquad (2)$$

where n and V_T are the sub-threshold slope factor and the thermal voltage, respectively. Assume that the current gain errors between MN2 and MN3 and between MP3 and MP4 are δ_n and δ_p, respectively. Then, $I_1 + I_2$ can be expressed as

$$I_1 + I_2 = (2 + \delta_n)(1 + \delta_p)I_2. \qquad (3)$$

Because V_{FB} is equal to $R_2V_{OUT}/(R_1+R_2)$, V_{OUT} can be expressed as

$$V_{OUT} \approx A_G\{V_{REF} - nV_T \ln(1 + 2\delta_p + \delta_n)\}, \qquad (4)$$

where A_G is $(R_1+R_2)/R_2$. When δ_n and δ_p are zero, V_{OUT} is equal to A_GV_{REF}. Therefore, the accuracy of V_{OUT} is determined by that of current mirrors. The high accuracy of the current mirror can be achieved using cascode current mirror.

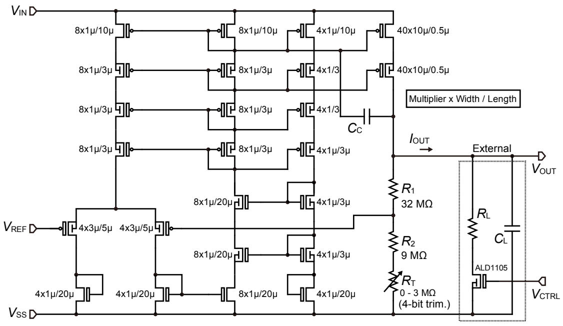

Fig. 3 Complete schematic of our proposed LDO.

Figure 3 shows a complete schematic of the proposed SB-LDO. The α was set to 1000. A low-power voltage reference circuit (VRC) is also implemented using [5]. The VRC generates V_{REF} with nano-watt power dissipation. To ensure the reliability against high input voltage, the thick gate-oxide MOSFETs are employed in cascode connection.

3. Measurement results

A prototype chip was fabricated with a 0.18-µm 1P6M CMOS process with deep n-well option. The 3.3-V tolerant MOSFETs were used. Figure 4 (a) shows a chip micrograph (area: 0.13 mm^2). Figure 4 (b) shows measured distribution of V_{OUT} before and after trimming in ten samples (V_{IN} = 4.5 V). After trimming, the mean μ, the standard deviation σ, and the coefficients of variation σ/μ, were 4.2 V, 21 mV, 0.50%, respectively.

Figure 5 (a) shows measured V_{OUT} as a function of V_{IN} in ten samples (I_{OUT} = 0 A). V_{OUT} was settled to 4.2 V when V_{IN} exceeded 4.2 V. The line regulation was 0.12%/V in the input range from 4.2 to 5.0 V. Figure 5 (b) shows measured input current I_{IN} including the current dissipation of VRC as a function of V_{IN}. Because of the input voltage error in DA ($V_{FB} \neq V_{REF}$), large I_{IN} flowed when V_{IN} was smaller than 4.2 V. However, I_{IN} was settled to about 100 nA in a steady state. The maximum quiescent I_{IN} was 151 nA. The proposed SB-LDO performed highly accurate and ultra-low power operation in quiescent condition. Figure 5 (c) shows measured error of V_{OUT} as a function of I_{OUT}. The maximum I_{OUT} was 1 and 6.8 mA when V_{IN} was 4.25 and 5.0 V, respectively. Figure 5 (d) shows measured I_{IN} and current use efficiency (Eq. (1)) as functions of I_{OUT}. The SB-LDO achieved 50 and 90% efficiency when I_{OUT} was 100 nA and 1 µA, respectively.

Figures 6 (a) and (b) show the measured transient waveforms and PSRR. R_L and C_L were set to 47.9 kΩ and 10 µF. We changed I_{OUT} dynamically by turning on and off the external switch with V_{CTRL} (see Fig. 3). We confirmed that V_{OUT} was stable against large load-current change. The measured PSRR was lower than –30dB when the input frequency was higher than 1 kHz. Table I summarizes the performance. The measurement results demonstrated that the SB-LDO achieved low-dropout, highly efficient, and stable operation.

4. Conclusion

A highly accurate and efficient SB-LDO was presented. The measurement results demonstrated that the proposed SB-LDO achieved 4.2-V output, 1-mA output current with 4.25-V input and 1% error, 151-nA quiescent current, and 90% current use efficiency with 1-µA output current.

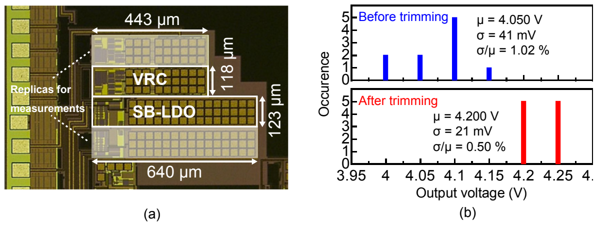

Fig. 4 (a) Chip micrograph and (b) measured distribution of V_{OUT} in ten samples (V_{IN} = 4.5 V).

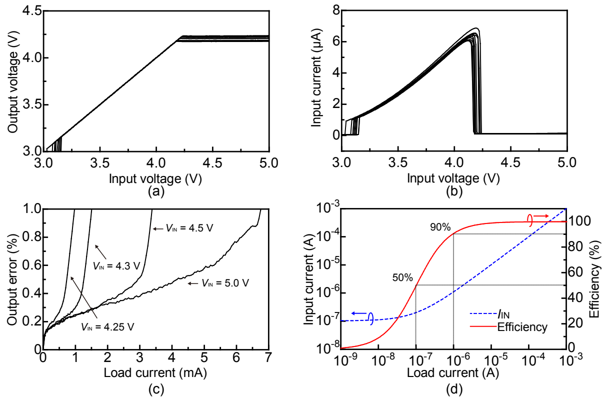

Fig. 5 Measured (a) V_{OUT} and (b) I_{IN} as functions of V_{IN} in ten samples (I_{OUT} = 0 A), (c) output error, and (d) I_{IN} and current use efficiency as functions of I_{OUT} (V_{IN} = 4.5 V).

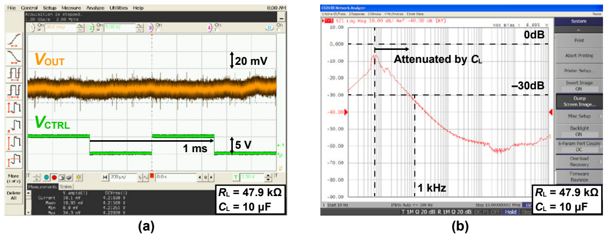

Fig. 6 Measured (a) transient waveforms and (b) PSRR.

Table I Performance summary.

Reference	This work	[3]
Technology	0.18-µm	0.5-µm
Area	0.13 mm^2	0.16 mm^2
V_{IN}	4.25 – 5.0 V	4.3 V
V_{OUT}	4.2 V	4.2 V
I_Q	< 151 nA	N / A
Max I_{OUT} (V_{IN})	1 mA (4.25 V)	3 mA (4.3 V)
Efficiency	> 90% (I_{OUT} > 1 µA)	(89.7%, power eff.)

Acknowledgements

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