A Self-Biased Low-Dropout Linear Regulator for Ultra-low Power Battery Management

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Abstract
This paper presents a self-biased low-dropout linear regulator (SB-LDO) for ultra-low power battery management. The SB-LDO employs a current feedback circuit to achieve highly accurate and efficient operation. Measurement results demonstrated that the proposed SB-LDO operates with ultra-low quiescent current of 151 nA. The maximum output current was 1 mA, when the input and output voltage were 4.25 and 4.16 V, respectively.

1. Introduction
Energy storage devices are an indispensable component for next generation power-aware small-sized energy harvesting applications [1]. A thin film Li-ion secondary battery is a good candidate for storing harvested energy [2]. However, a Li-ion battery must be protected from overcharge voltage (e.g., typical charging voltage is 4.2 V), the charging voltage must be carefully regulated. Figure 1 shows a block diagram of the battery charger. Low-dropout regulators (LDOs) are commonly used for battery charging applications [1]. A thin film Li-ion secondary battery is a good candidate for storing harvested energy [2]. However, because a Li-ion battery must be protected from overcharge voltage [3, 4]. Therefore, a highly accurate and efficient LDO is strongly required for ultra-low power Li-ion battery management.

In this paper, we propose a self-biased (SB) LDO employing a current feedback technique to achieve highly accurate, ultra-low quiescent current, and highly efficient voltage regulation. Details of the circuit are as follows.

2. Architecture and circuit design
Figure 2 shows a simplified schematic of the proposed SB-LDO. It consists of a differential amplifier (DA), current feedback circuit (CFC), and output stage. Note that, in our SB-LDO, a current reference circuit to bias the DA is not used. When output current \( I_{\text{OUT}} \) changes, bias currents in the LDO adaptively change to maintain \( V_{\text{FB}} = V_{\text{REF}} \), where \( V_{\text{FB}} \) and \( V_{\text{REF}} \) are the feedback and reference voltages. The circuit achieves high accuracy and ultra-low quiescent current by using a feedback loop with CFC. Details of the operation are as follows.

The current mirror gains of the nMOS (MN2:MP3) and pMOS (MP3:MP4:MP5) transistors are set to 1:2 and 1:1:α, respectively. When \( I_{\text{OUT}} \) becomes large, the output voltage \( V_{\text{OUT}} \) and the feedback voltage \( V_{\text{FB}} \) decrease. Then, \( I_2, I_3, I_{\text{OUT}} \) and \( I_{\text{FB}} \) increase. Therefore, \( V_{\text{OUT}} \) and \( V_{\text{FB}} \) increase to maintain \( V_{\text{FB}} = V_{\text{REF}} \).

In a steady state, \( I_1, I_2, \) and \( I_3 \) settle to \( 2I_1 = 2I_2 = I_3 = (I_{\text{OUT}} + I_{\text{FB}})/\alpha \), where \( I_{\text{FB}} \) is the current flowing in the feedback resistors \( R_1 \) and \( R_2 \). The current use efficiency of the proposed SB-LDO can be defined as

\[
\frac{I_{\text{OUT}}}{I_{\text{IN}}} = \frac{I_1 + I_2 + I_3 + 2I_1 + I_{\text{FB}}}{I_1 + I_{\text{FB}}} = \frac{\alpha}{\alpha + 2} \cdot \frac{I_{\text{OUT}}}{I_{\text{FB}}}. \quad (1)
\]

Therefore, the larger the \( \alpha \), the higher the efficiency.

In the sub-threshold region of MOSFETs, \( I_2 \) can be expressed as

\[
I_2 = \frac{I_1 + I_2}{1 + \exp((V_{\text{REF}} - V_{\text{FB}})/(nV_T))}, \quad (2)
\]

where \( n \) and \( V_T \) are the sub-threshold slope factor and the thermal voltage, respectively. Assume that the current gain errors between MN2 and MN3 and between MP3 and MP4 are \( \delta_n \) and \( \delta_p \), respectively. Then, \( I_1 + I_2 \) can be expressed as

\[
I_1 + I_2 = (2 + \delta_n)I_1 + \delta_p. \quad (3)
\]

Because \( V_{\text{FB}} \) is equal to \( R_2V_{\text{OUT}}/(R_1+R_2) \), \( V_{\text{OUT}} \) can be expressed as

\[
V_{\text{OUT}} = A_C(V_{\text{REF}} - nV_T\ln(1 + 2\delta_n + \delta_p)). \quad (4)
\]

where \( A_C \) is \( (R_1+R_2)/R_2 \). When \( \delta_n \) and \( \delta_p \) are zero, \( V_{\text{OUT}} \) is equal to \( A_CV_{\text{REF}} \). Therefore, the accuracy of \( V_{\text{OUT}} \) is determined by that of current mirrors. The high accuracy of the current mirror can be achieved using cascode current mirror.
Figure 3 shows a complete schematic of the proposed SB-LDO. The α was set to 1000. A low-power voltage reference circuit (VRC) is also implemented using [5]. The VRC generates $V_{\text{REF}}$ with nano-watt power dissipation. To ensure the reliability against high input voltage, the thick gate-oxide MOSFETs are employed in cascode connection.

3. Measurement results

A prototype chip was fabricated with a 0.18-μm 1P6M CMOS process with deep n-well option. The 3.3-V tolerant MOSFETs were used. Figure 4 (a) shows a chip micrograph (area: 0.13 mm²). Figure 4 (b) shows measured distribution of $V_{\text{OUT}}$ before and after trimming in ten samples ($V_{\text{IN}} = 4.5$ V). After trimming, the mean $\mu$, the standard deviation $\sigma$, and the coefficients of variation $\sigma/\mu$ were $4.2$ V, $21$ mV, and $0.50\%$, respectively.

Figure 5 (a) shows measured $V_{\text{OUT}}$ as a function of $V_{\text{IN}}$ in ten samples ($I_{\text{OUT}} = 0$ A). $V_{\text{OUT}}$ was settled to 4.2 V when $V_{\text{IN}}$ exceeded 4.2 V. The line regulation was $0.12\%$/V in the input range from 4.2 to 5.0 V. Figure 5 (b) shows measured input current $I_{\text{IN}}$ including the current dissipation of VRC as a function of $V_{\text{IN}}$. Because of the input voltage error in DA ($V_{\text{FB}} \neq V_{\text{REF}}$), large $I_{\text{IN}}$ flowed when $V_{\text{IN}}$ was smaller than 4.2 V. However, $I_{\text{IN}}$ was settled to about 100 nA in a steady state. The maximum quiescent $I_{\text{IN}}$ was 151 nA. The proposed SB-LDO performed highly accurate and ultra-low power operation in quiescent condition. Figure 5 (c) shows measured error of $V_{\text{OUT}}$ as a function of $I_{\text{OUT}}$. The maximum $I_{\text{OUT}}$ was 1 and 6.8 mA when $V_{\text{IN}}$ was 4.25 and 5.0 V, respectively. Figure 5 (d) shows measured $I_{\text{IN}}$ and current use efficiency (Eq. (1)) as functions of $I_{\text{OUT}}$. The SB-LDO achieved 50 and 90% efficiency when $I_{\text{OUT}}$ was 100 nA and 1 μA, respectively.

Figures 6 (a) and (b) show the measured transient waveforms and PSRR. $R_L$ and $C_L$ were set to 47.9 kΩ and 10 μF. We changed $I_{\text{OUT}}$ dynamically by turning on and off the external switch with $V_{\text{CTRL}}$ (see Fig. 3). We confirmed that $V_{\text{OUT}}$ was stable against large load-current change. The measured PSRR was lower than –30dB when the input frequency was higher than 1 kHz. Table I summarizes the performance. The measurement results demonstrated that the SB-LDO achieved low-dropout, highly efficient, and stable operation.

4. Conclusion

A highly accurate and efficient SB-LDO was presented. The measurement results demonstrated that the proposed SB-LDO achieved 4.2-V output, 1-mA output current with 4.25-V input and 1% error, 151-nA quiescent current, and 90% current use efficiency with 1-μA output current.

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References