Extended Abstracts of the 2016 International Conference on Solid State Devices and Materials, Tsukuba, 2016, pp465-466

K-1-01(Invited)

Electrostatic perturbations from TSV processing during 3D integration of advanced CMOS Technologies

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Abstract

Due to complex processing TSV integration can perturb the functionality of the underlying CMOS technology. In this paper we summarize the results on the electrostatic perturbations caused by TSV on devices in proximity and describe characterization techniques to detect them. Potential issues in packaging and wafer to wafer bonding are identified and potential solutions are demonstrated.

1. Introduction

Through Silicon Via (TSV) are the basic elements for achieving 3D integration, essential for improved system performance in the era of saturating transistor performance. They provide the pathway to providing power as well as signal communication among the various layers in a 3D chip. Often, these TSVs are introduced into advanced CMOS technology layers that are optimized for yield and performance as stand-alone 2D chips (Fig1). However, the high aspect ratios involved in the TSV along with challenges introduced due to process can perturb the functionality of the CMOS layer. In this paper, we discuss such a perturbation, one that is related to electrostatic charges resulting from TSV process.

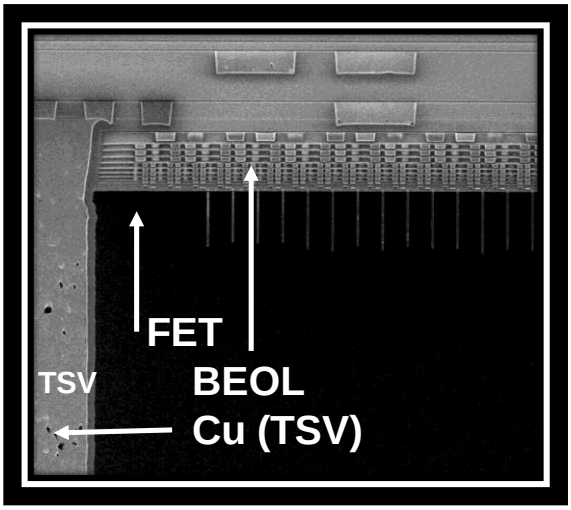

Fig 1. Typically the TSV is introduced into existing CMOS chips whose FETs and wiring are individually optimized for 2D performance

2. TSV interaction to Devices

Initial attempts at making copper filled TSV were thwarted by the severe thermal expansion mis-match between copper and silicon resulting in extrusions. Such structural issues were addressed with improved adhesion to the liners and 'bottoms-up' plating of Cu. Although the extrusions were prevented the stress resulted in the change in device characteristics in proximity to TSV. Such perturbations are typically addressed via suitable choice of 'keep-out-zone', where devices are forbidden [1].

Such stresses typically affect the channel mobility resulting in changes to the device currents (saturation current, Ion or the linear current, Idlin). For e.g., the radially tensile stress from the TSV exerts a tangential compressive stress resulting in the reduction of the ion of NFET1 (Fig 2) while no change is observed in the threshold voltage (Vt). However, if there are positive charges present in proximity, either through mobile ion contamination [2] or copper extrusions [3], the threshold voltage is changed (Fig 3).

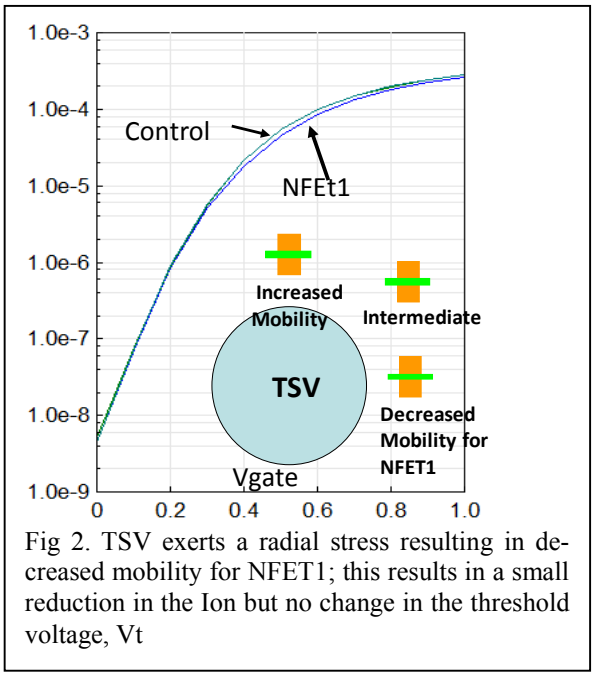

Fig 2. TSV exerts a radial stress resulting in decreased mobility for NFET1; this results in a small reduction in the Ion but no change in the threshold voltage, Vt

While changes in mobility are problematic for accurate device models essential for circuit design, mobile ion contamination causes a more fundamental issue for proper functioning of the chip as the ions are mobile at chip operating temperature resulting in unpredictable circuit function in the field.

3. Characterisation and Mitigation

While the presence of ions such as Cu, Na, K are easily detected by analytical techniques such as SIMS, it is much

more suitable to detect them via electrical characterization techniques that have the added advantage of being non-destructive. Id-Vg curves such as in Fig 3 can show the presence

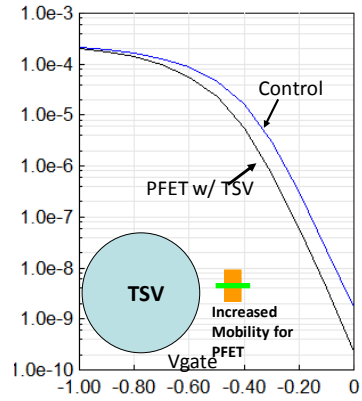

Fig 3. In the presence of charge, the PFETs show a change in the threshold characteristics, with relatively little change in the on-current; the stress model would predict an increased mobility for this configuration

of charge, it cannot identify the species or give an idea about their concentration. C-V techniques, while sensitive to the presence of charge, again, do not have any specificity to the type of mobile ions or their concentrations. We have adapted the technique of triangular voltage sweeps (TVS) to address this issue Fig 4.

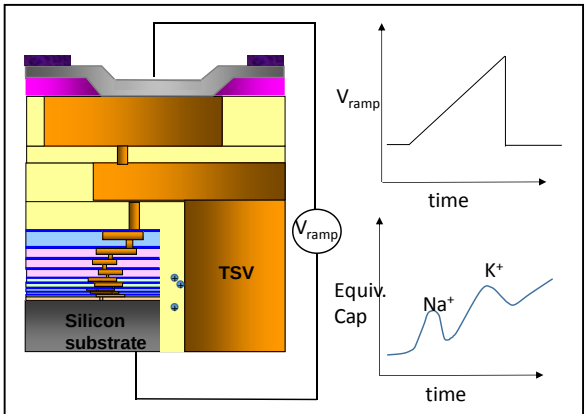

Fig 4. The TVS spectrum is recorded by applying a ramp voltage and recording the current, typically expressed as an equivalent capacitance; lighter ions such as Na^+ typically show up earlier and have sharper peaks than heavier ions such as K^+ or Cu^{++}

This technique was demonstrated to show specificity to both mobile ions such as Na and K coming from CMP chemistries as well as Cu extrusions from TSV[3]. When unable to change CMP buffering agents, the primary source of mobile ions, cleaning with chelating agents were used to remove the impact of mobile ions. Cu migrations were stemmed by improved integration of the liner materials for the TSV.

4.0 Impact from thinning and packaging

Besides the potential for the migration of ions from BEOL 3D integration has another significant challenge posed by the

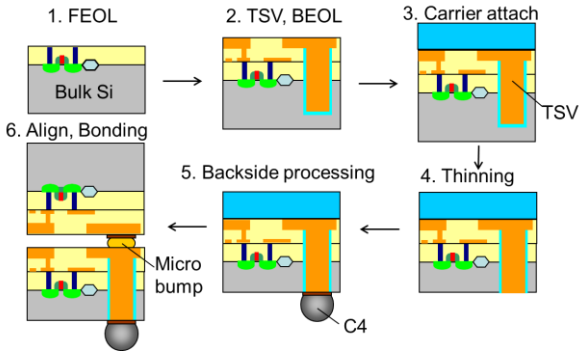

Fig.5 To complete the 3D integration, the 2D wafer is thinned along with backside processing, a potential source for the introduction of ions. This can pose additional sources of perturbation to devices.

thinning and the subsequent assembly process (Fig 5). This involves back-side thinning and subsequent backside processing, during which the device side has a direct pathway for mobile ion migration, via the TSV dielectric. Wherever possible the buffering agents for CMP must have low ionics to prevent such perturbations as ions can easily migrate along the TSV dielectric from back-side to the device side. Alternatively, gettering implants can be used that can bind the mobile ions and prevent their migration to sensitive device areas.

3. Conclusions

Electrostatic perturbations arising from TSV processing has been described. Electrical characterization techniques for identifying the issue along with its quantification has been proposed. Potential sources of such effects in thinning and packaging are identified and mitigation strategies were discussed.

Acknowledgements

The authors would like to thank all members of the 3D integration team and 300 mm advanced fabrication facility in East Fishkill, NY for the samples and SIMS analysis.

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3. [3] C. Kothandaraman et al. in "Triangular voltage sweep characterization for TSV reliability" **Proc. of International Reliability Physics Symposium (IRPS), (2016).**