Extended Abstracts of the 2016 International Conference on Solid State Devices and Materials, Tsukuba, 2016, pp467-468

K-1-02

Evaluation of Depth-dependent TSV-liner Interface States Using Multi-well Structured TSV and Charge Pumping Technique

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Abstract

We have proposed a novel evaluation method for depth-dependent TSV-liner interface states with multi-well structured TSV and charge pumping technique. As results, we successfully observed the interface states distribution of TSV sidewall along depth direction. Uniform TSV liner SiO_2 and Ti barrier were required to suppress charge pumping current and to realize highly reliable and high performance 3D-IC with TSVs.

1. Introduction

Three dimensional stacked IC (3D-IC) has attracted much attention since it can improve the IC performance without further scaling down of transistor size. 3D-IC consists of vertically stacked and electrically connected chips with lots of through-Si vias (TSVs). Although it is well known that TSVs give negative impacts on transistors around the TSV with mechanical stress, it is also concerned that TSVs also affect the transistors with extrinsic currents generated from interface states at TSV liner like charge pumping currents. Therefore, it is very important to evaluate the interface state at the TSV liner. In general, it is considered that interface states density varies in accordance with the TSV depth and this is attributed to both non-uniform thickness and interface quality of TSV liner. However, in previous reports [1][2], distribution of interface states along TSV depth was not investigated at all. In this study, a novel test vehicle having TSVs with multi-well structure was fabricated and the interface states at TSV liner along the TSV depth direction was evaluated in detail.

2. Fabrication of Multi-well Structured TSV

We evaluated the interface states at TSV liner along the TSV depth direction using multi-well structured TSVs, as shown in Fig. 1. In the multi-well structured TSV, both nMOSFET and pMOSFET were vertically and simultaneously formed along TSV sidewall. Charge pumping current of each MOSFET was measured and depth-dependent interface states were precisely extracted.

Figure 2 showed fabrication flow of the test structure with multi-well structured TSV. First, a IC chip with multi-well structured TSVs was flip-chip bonded to Si interposer with Cu/Sn microbumps. Then, the IC chip was thinned to 34-μm thick by mechanical grinding and chemical mechanical polishing (CMP). After SiO_2 deposition, via holes were formed from backside of the IC chip using Bosch process with inductively coupled plasma reactive ion etching (ICP-RIE). Next, TSV liner SiO_2 was deposited by plasma enhanced chemical vapor deposition (PE-CVD) at 200 degree C using TEOS and O_2. And bottom SiO_2 was removed by anisotropic etching. After Ti barrier layer and Cu seed layer deposition, TSV was filled with Cu by bottom-up plating. The Cu overburden and Ti barrier on the backside surface were removed by Cu-CMP and wet etching, respectively. The TSVs diameter and depth were 7 μm and 25 μm. The thickness of TSV liner SiO_2 and barrier layer on the back surface of IC chip were 4 μm and 100 nm, respectively. Figure 3 shows the cross-sectional schematic image of the test structure. In this study, the multi-well structured TSV was composed of N^+-diffusion region, P-well, deep N-well, and P-substrate, as shown in Fig. 3.

3. Experimental Results and Discussion

Figure 4 showed I-V characteristics of MOS diodes formed in the multi-well structured TSV. There were four kinds of MOS diodes composed of four impurity regions mentioned above. TSV voltages at current sign inversion decreased for the MOS diode formed with N^+-diffusion region at deeper TSV. This result indicated the TSV liner SiO_2 and/or Ti barrier closed to via bottom were not good characteristics.

Figure 5(a) and (b) showed the Id-Vg characteristics of nMOSFET and pMOSFET formed along TSV sidewall. In Fig. 5(a), TSV, N^+-diffusion, P-well, and deep N-well corresponded to gate, drain, body, and source of the nMOSFET, respectively. In Fig. 5(b), TSV, P-well, deep N-well, and P-sub corresponded gate, drain, body, and source of the pMOSFET, respectively. Both MOSFETs showed conventional Id-Vg behaviors, indicating that the depth-dependent interface states were evaluated by charge pumping technique.

Finally, the charge pumping currents were measured for the MOSFETs formed on TSV sidewall. Figure 6(a) showed a pulse waveform applied to the multi-well structured TSV to measure the charge pumping currents between TSV liner SiO_2 and each well. Figure 6(b) showed measured charge-pump currents for different base voltages of TSV (V_{base}). Here, I_{cp1} was charge-pump current between TSV and N^+-diffusion/P-well. I_{cp2} was charge-pumping current be-

tween TSV and P-well/deep N-well. I_{cp3} was charge-pumping current between TSV and deep N-well/P-sub. The charge pumping currents showed quite different behaviors along TSV depth. In the case of I_{cp2} and I_{cp3}, two current peaks were observed. Right and left peaks of I_{cp2} were generated from interface states between TSV liner SiO_2 and P-well and between TSV liner SiO_2 and deep N-well, respectively. Right and left peaks of I_{cp3} were generated from interface states between TSV liner SiO_2 and P-sub and between TSV liner SiO_2 and deep N-well, respectively. In contrast, in the case of I_{cp1}, although it was reasonable that there was a peak at base voltage around -0.3 V, it was not reasonable that there was also a peak around deep base voltages in spite of high doping concentration of N^+-region. This result indicated the TSV liner SiO_2 and/or Ti barrier around N^+-region were not good characteristics. Consequently, distribution of interface states along TSV depth was not uniform and these results can be evaluated with the multi-well structured TSV and charge pumping technique.

4. Conclusion

A novel multi-well structured TSV was proposed. The interface states of TSV liner along depth direction were successfully evaluated with the multi-well structured TSV and charge pumping tecnique. This evaluation method becomes a versatile tool to fabricate highly reliable and high performance 3D-IC with TSVs.

Acknowledgment

This work was partially supported by JSPS KAKENHI Grant Number 15H01812. This device was fabricated in Micro/Nano-machining research and education Center (MNC) at Tohoku University.

References

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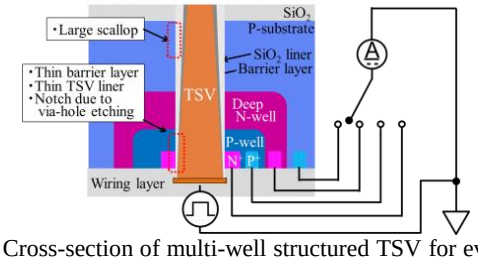

Fig. 1. Cross-section of multi-well structured TSV for evaluation of depth-dependent TSV liner interface states.

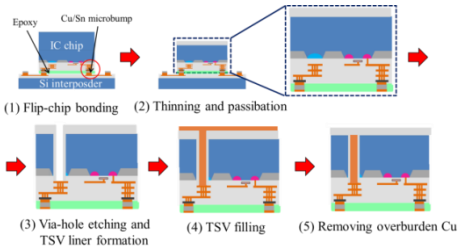

Fig. 2. Fabrication flow of the test structure with multi-well structured TSV.

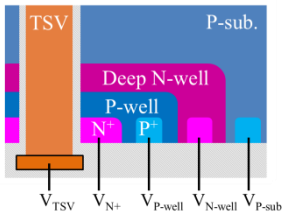

Fig. 3. Schematic cross-sectional drawing of the fabricated test structure with multi-well structured TSV.

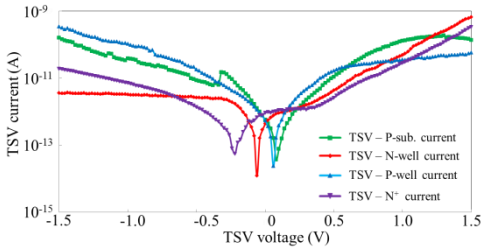

Fig. 4. *I-V* characteristics of MOS diode formed in the multi-well structured TSV.

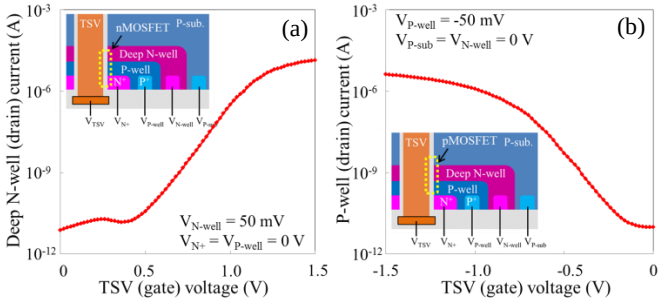

Fig. 5. I_d-V_g characteristics of (a) nMOSFET and (b) pMOSFET formed in the multi-well structured TSV.

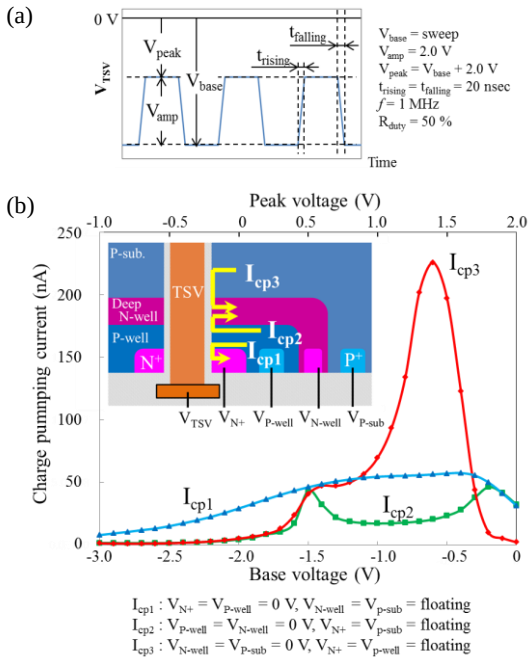

Fig. 6. Applied TSV voltage waveform and measurement results of charge pumping currents between TSV liner SiO_2 and each well.