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Superiority of In-Stack Decoupling Capacitor for 3D-LSI with Wide I/O Data Bus

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Abstract

Power noise reduction in 3D LSI by in-stack decoupling capacitors (DECAPs) is demonstrated with a three-tier demonstrator having vertical data bus transceivers between memory and logic chips. In-stack evaluation circuitry on a middle tier (Si interposer) captured power voltage waveforms during chip-to-chip data communication. The in-stack DECAPs in arrays on the Si interposer and discrete ceramic capacitors on the organic interposer of a ball-grid array package are compared. Silicon measurements reveal it that the in-stack DECAPs reduce AC components of power noise over a 5 times wider frequency range even with 1/10 of total capacitance, in comparison to the package DECAPs.

1. Introduction

High-performance LSIs demand ultra-wide data communication between processor cores and memory macros, for enabling such as massive data processing and advanced machine learning. In line with this scenario, the state-of-the-art GPUs are integrated with multiple processor and memory modules on a Si interposer.

Regarding data communications, it is of prime importance to reduce data path length. This can concurrently improve energy efficiency and achieve faster data transfer. One of promising techniques is through silicon via (TSV) based three-dimensional (3D) Si integration, not just minimizing the data path lengths but also maximizing the number of vertical signal channels.

To realize high-performance 3D-LSI, noise problems should be addressed. The power current density becomes larger with the higher level of integration, and enlarges power noise that can potentially lead to the degradation of system performance or even malfunction of an entire system often by electromagnetic interference (EMI). Our previous research shows that a decoupling capacitor (DECAP) in 3D LSI can potentially mitigate noise problems in terms of EMI [1]. This paper experimentally investigates the validity of DECAPs on a Si interposer within 3D chip stacking, with quantitative comparisons to conventional ones normally built on an organic package substrate.

In this study, three-tier 3D-LSI samples with ultra-wide data communication bus are used [2]. The effects of power noise reduction are measured with in-stack noise monitoring technique.

2. Three-tier stacked LSI sample

Fig. 1 shows an overall structure of 3-tier stacked LSI chips. The stack consists of top memory, bottom logic and active Si interposer between them. These 3 dice are manufactured by 90 nm CMOS process, and the chip size each is 9.9 mm x 9.9 mm. The three tiers are vertically connected by TSVs and μ-bumps, and mounted on an organic substrate, as depicted in Fig. 2(a). The logic and Si interposer tiers have TSVs fabricated with so-called via-last processing. The Si substrate is thinned from its backside up to the whole thickness of 50 μm. Then, TSVs are etched by Bosch process and electroplated with Cu for filling. Fig. 2(b) shows a cross-sectional photo of the stack including TSVs and micro-bumps. The stacked sample is mounted on a 527 pin BGA package substrate and assembled with flip-chip bumps.

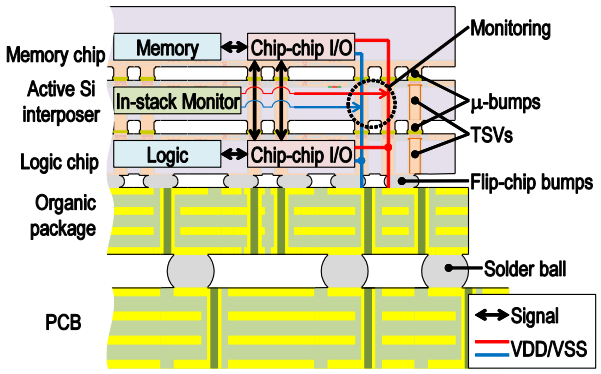


Fig. 1. 3-tier stacked LSI chips with in-stack monitor.

The stacked sample has a ultra-wide communication bus [2] which vertically connects logic and memory chip through TSVs on an active Si interposer. The vertical chip-to-chip communication has the wide-I/O bus width of 4096 bits split into 8 banks of 512 bits each. The chip-to-chip communication circuitry has an independent power delivery network in the stack, which can be monitored by in-stack monitor circuitry [3] on the active Si interposer.

We have evaluated 3 types of chip stacks with different DECAP structures as defined in Fig. 3. The “no DECAP” excludes intentional capacitors (Fig. 3(a)). The “package DECAP” has 15 x 0.1 μF discrete chip capacitors (1.5 μF in total) on the solder-ball side of the BGA package (Fig. 3(b)). The “in-stack DECAP” has on-chip MIM and MOS capacitors (128 nF in total) processed on the Si interposer (Fig. 3(c)).

3. In-stack evaluation

The in-stack monitoring circuitry on the Si interposer enables sampling and digitizing voltage waveforms at the power line (V_{DD}) nodes of vertical bus data transceivers.

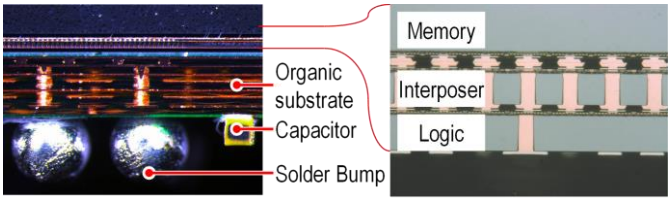
Figure 4 compares the V_{DD} waveforms among the three DECAP structures at the bus operating frequency of 10 MHz. In comparison to "no DECAP", "in-stack DECAP" exhibits noise attenuation over the clock period of bus operation, with significant reduction of the first voltage drop right after the clock edge (as seen in the magnified plot of Fig. 4(b)). In contrast, "package DECAP" shows slight attenuation to the first drop, and the waveform is followed by resonating voltage variation that causes undesirable peaks.

Figure 5 shows the frequency components derived from the measured waveforms. Fig. 5(b) only includes the integer harmonics among them for the operating frequency at 10 MHz. "In-stack DECAP" suppresses the noise components stably over a wide frequency range. In contrast, "package DECAP" is effective within 70 MHz while enlarging the high order harmonics.

It should be noted that "in-stack DECAP" sustains the noise suppression over five times wider frequency, even with less than one-tenth capacitance of "package DECAP." The relative inefficacy in the low frequency range of "in-stack DECAP" can be compensated by "package DECAP" if both DECAPs concurrently exist. In-stack capacitors are of essential significance for achieving signal and power integrity of 3D LSI featuring high-frequency and very widely parallel bus transceivers.

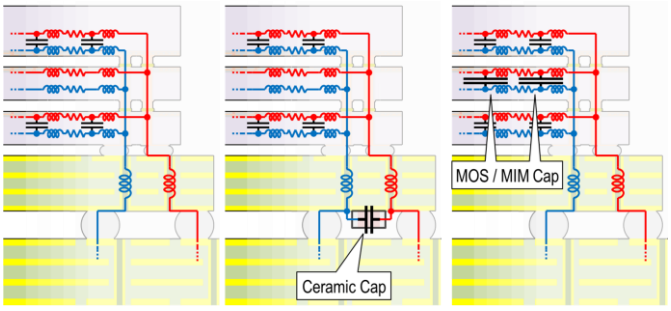
4. Conclusions

Power noise reduction by DECAPs on a Si interposer in 3D chip stacking is demonstrated with three-tier TSV based demonstrators. The in-stack DECAPs accomplish the signal and power integrity of 3D LSI at a superior level to conventional 2D packaged chips, and essentially support the high speed and very wide bandwidth operation of 3D stacked circuits.



(a) (b)

Fig. 2. Cross-sectional view of (a) packaged sample and (b) TSVs and micro-bumps.



(a) (b) (c)

Fig. 3. TEG design of (a)no DECAP TEG, (b) package DECAP TEG, and (c) in-stack DECAP TEG

Acknowledgements

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References

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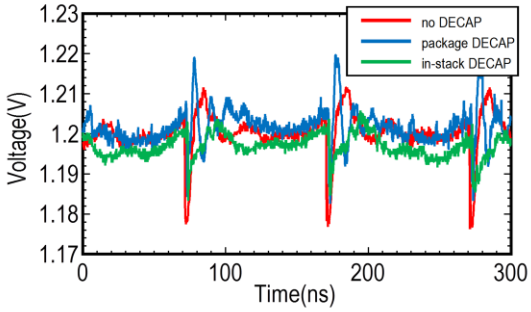
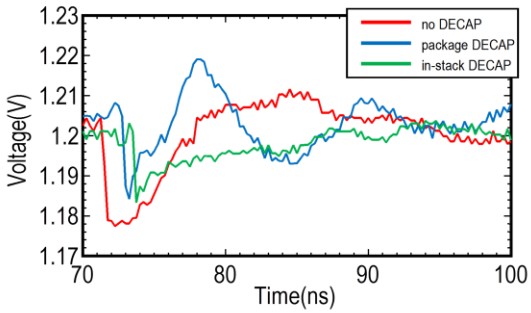
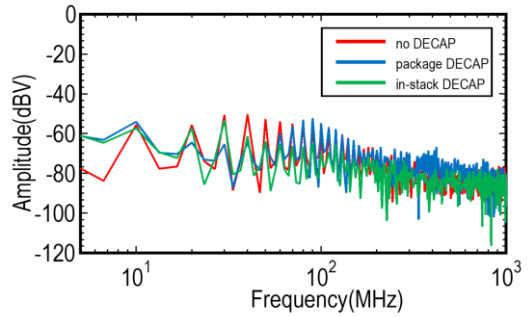


(a)

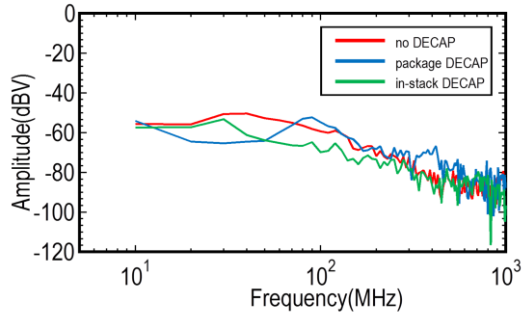


(b)

Fig. 4. (a)Measured V_{DD} waveform and (b) magnified view.



(a)



(b)

Fig. 5. (a)Frequency component of measured V_{DD} waveform and (b) peak components plot.