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CMP – Stack Trek

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Abstract

From its introduction, in 1983, in semiconductor manufacturing, Chemical Mechanical Planarization (CMP) was key enabler technology for building stacks. Starting with dielectric planarization in order to allow metal interconnect stacking and going to high level system integration by stacking of heterogeneous devices, the CMP follows the trek to perfect planarization final frontier. In this paper we will present this stack trek.

1. Introduction

On 1 December 1957, physicist Jean Hoerni conceived the planar process, a technique used to manufacture essentially all silicon transistors and micro- chips today [1]. Eight years later, Gordon E. Moore, working for Fairchild Semiconductor, predicted, based on its company production, that the number of components on an integrated circuit will double every year for next ten years and will go from about 64 to 65,000 [2]. In 1975, Moore, now at Intel, revised his first prediction: doubling the transistor number will see a two-year cycle [3]. He argued that three factors contributed to the trend:

- increasing chip area,
- decreasing component size, and
- "device cleverness," in order to decrease the unused area between transistors.

If in the early days, what we can call today Moore's Law 1.0 "scaling up" by adding more components to a chip, was dominant, over the last few decades, progress in the semiconductor industry was driven by "scaling down" in a 2.0 version of Moore's law. Over the years, semiconductor manufacturers could increase chip transistor density by miniaturizing the transistor size, while keeping cost per area constant. This cost per transistor reduction was possible with, especially, lithography help but today the trend is ending as lithography costs are highly increasing for advanced nodes [4].

As stated by ITRS Roadmap we are entering now in a, so called, Moore 3.0 law version, the More the Moore era: "The combination of 3D device architecture and low power devices will usher in a new era of scaling identified in short as "3D Power Scaling." [5]. After reducing transistor costs, platform-level costs and total system integration should be key drivers for next years in semiconductor industry.

2. CMP

Introduced in 1983 by IMB scientist engineer Klaus Beyer, [6] Chemical Mechanical Planarization (CMP) was an enabling technology for semiconductor manufacturing. Its first application in those first days were to "contribute to device cleverness" by reducing unused area between transistors. In that period IBM was switched its technology for glass isolation trench from 2 µm to 1.5 µm width. That miniaturization had an issue with 1.5 µm trench not well filled and also unwanted mounds at random locations of the wafers. Beyer, who worked on that time on a silicon surface cleaning process post polishing, decided to polish the trench isolation test wafer with the reflowed glass fill that had the unwanted mounds on it, along with polishing a batch of prime silicon wafers at discovered uniform wafers with well planarized surfaces.

So if the P in CMP is sometimes used to denote polishing, which may imply only material removal as in the case of a featureless blanket film, in contrast, "planarization" explicitly refers to the ultimate role of CMP in achieving the wafer- and die-level surface planarity across widely varying pattern sizes and densities. On the other side, "chemical-mechanical" words indicates that there is a strong synergy between those two actions and the control of this synergy is the key for success of the CMP process.

Second application of the CMP concerned decreasing component size: having a planar oxide surface over the etched aluminum lines enabled lithography to have good depth of field control for vertical etched vias that could be filled with CVD tungsten and then etched back. The nanoscale surface topographic uniformity that is essential to overcome the depth-of-focus limitations of the lithography techniques used to pattern the device structures can only be achieved by the CMP process, therefore CMP became mandatory for submicronic nodes. So, if lithography enabled scaling, it needs the help of the Chemical Mechanical Planarization which, through high level surface flattening, enabled stacking of multiple layers.

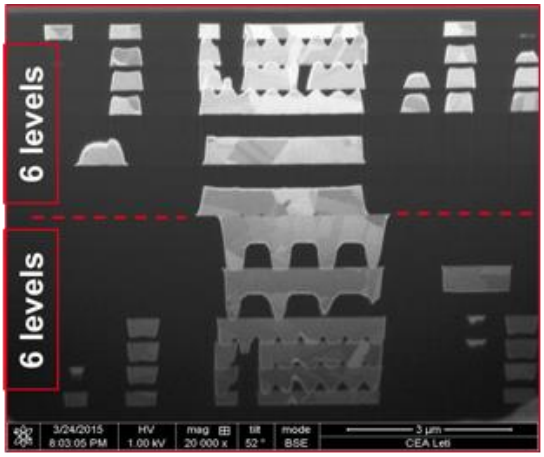
Finally, chemical selectivity against materials allowed CMP process to selectively remove metals, as tungsten and copper and therefore easily fabricate metal interconnects. This allowed, once again, to stack multiple levels of metal interconnects for advanced nodes transistors – 15 metal layers stacked in the IBM 22nm POWER8 chip.

3. 3D

As 3D (three-dimensional) integration was identified as solution to further power scaling through the possibility of shorter wiring and the associated potential benefits to resistivity, power consumption, delay, it also represents an enabling technology for improved integration of heterogeneous devices, which offers by the same, form-factor improvement. Hybrid bonding process with oxide / copper direct bonding allows the highest scalability of interconnect pitch [8]. For high-quality wafer bonding, excellent surface planarization is needed at all spatial wavelengths [9] therefore advanced CMP process should be developed in order to address aggressive

topography specifications.

Fig. 1 7 µm pitch copper-copper hybrid direct bonding of 300mm



wafers.

In this paper we will present the CMP stack trek from its stone age, when it enabled to reduce unused area between transistors through trench polishing, to future heterogeneous building blocks through wafer-to-wafer bonding, allowing complex systems integration by stacking different devices..

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