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III-V Nanowires and Nanofins: Growth, Etching, and Devices

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Abstract

III-V nanowires and nanofins grown via the vapor-liquid-solid (VLS) or selective area epitaxy (SAE) mechanism, and fabricated by metal-assisted chemical etching (MacEtch) will be presented, along with related devices.

1. Introduction

III-V compound semiconductor, due to its high mobility and versatile heterojunctions, has been considered as one of the highly promising candidates for beyond-silicon CMOS and high speed low power RF and logic applications [1]. Nanowires (NWs) and nanofins with their 3D cross-sections can greatly reduce the short channel effects that limit the scalability and linearity of various type of transistors.

In this talk, we first present a unique bottom-up growth method, selective lateral epitaxy (SLE) via the vapor-liquid-solid (VLS) mechanism using MOCVD, to form planar NW arrays for transistors with an inherent 3D channel. Selective area epitaxy of nanowires and nanofins on silicon and 2D van der Waals substrates will also be discussed. We then present a novel top-down fabrication method, metal-assisted chemical etch (MacEtch), to form extremely high aspect ratio atomically smooth nanofin arrays for finFETs.

2. General Instructions

Bottom-up grown planar GaAs nanowires for 3D transistors

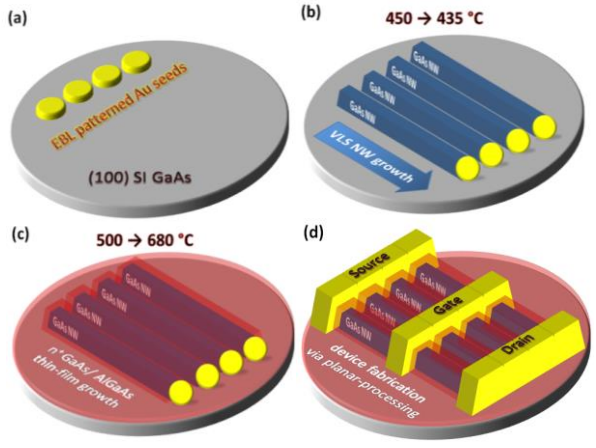

Fig. 1 Process flow for the growth and fabrication of planar GaAs NW HEMT with AlGaAs:Si carrier supplying layer and n^+GaAs cap.

III-V nanowires can be grown epitaxially along a particular crystal orientation in the plane of single crystal substrates, guided by metal catalyst nanoparticles via the VLS mechanism. By patterning the metal nanoparticles, under controlled growth conditions, the NWs can propagate laterally precisely positioned in selected locations with desired density; and the length of the NWs are determined simply by the growth time. Long and uniform planar GaAs NWs were assembled in perfectly parallel arrays to form double-channel T-gated NW array-based high electron mobility transistors (HEMTs), shown

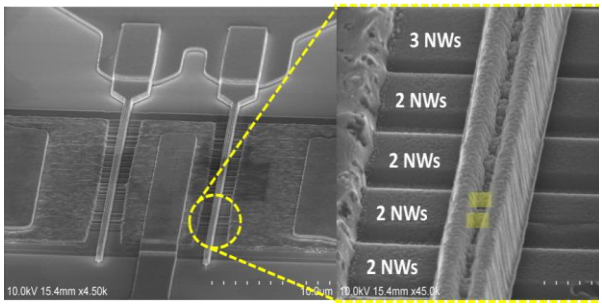

Fig. 2 SEM image of a fully fabricated double-channel T-gated GaAs/AlGaAs NW HEMT, with the NW-channel region zoomed in where the T-gate can be seen sitting atop groups of parallel NWs.

in Fig. 1, with excellent DC and RF performance [2,3]. By characterizing more than 100 devices on a 1.5 × 1.5 cm2 chip, we prove chip-level electrical uniformity of the planar NW array-based HEMTs and verify the feasibility of using this bottom-up planar NW technology for large-scale nanoelectronics.

SAE nanowires for heterogeneous integration

In contrast to VLS growth where metal nanoparticles define the location of the NWs, in SAE, the substrates are patterned by lithography, where NW grow in the unmasked areas and no growth takes place on top of the oxide mask in MOCVD. Ordered arrays of SAE grown GaAs, InP, GaP, as well as ternary III-V nanowires and nanofins have been demonstrated on Si (111) and van der Waals 2D substrates such as graphene. The effect of growth temperature, V/III ratio, growth rate, and doping on the morphology of the SAE nanostructures will be discussed.

Top-down etched nanowires and nanofins for HAR FETs

MacEtch is a wet but anisotropic etching method that defies textbook definition of wet etch. The etching reaction only occurs in the presence of the metal catalyst (Au, Pt, and CMOS compatible metals). This process eliminates dry etching-induced plasma damage, high energy ion implantation damage, and subsequent high-temperature annealing thermal budget, ensuring interface quality between the high-k gate dielectric and the fin channel in MOSFETs. InP junctionless FinFETs with record high aspect ratio (as high as 50:1), fabricated by inverse MacEtch (i-MacEtch), are demonstrated to have excellent SS and $I_{on/off}$, as well as decent I_{on} [5]. Fig. 3 shows an array of InP nanofins, where both ends of the fins are intentionally made wider than the center region to help reduce source/drain contact resistance. Fig. 4 shows one of the fully fabricated InP nanofin with width as narrow as 14 nm and a height of 700 nm in a uniform array.

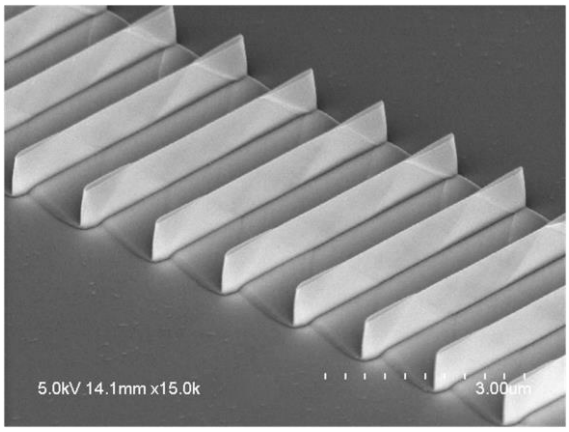

Fig. 3 SEM images of an array of InP fins formed by i-MacEtch.

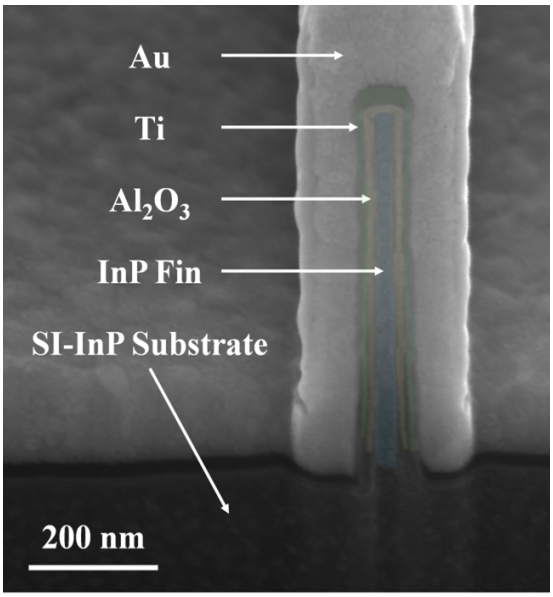

Fig. 4 SEM of a fully fabricated InP fin with fin width as narrow as 14 nm and height of 700 nm. Adapted from ref. [5].

3. Conclusions

Novel bottom-up growth and top-down fabrication nanotechnology enables the realization of 3D III-V transistors without suffering self-assembly related randomness or etching damage.

Acknowledgements

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References

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