Device and Circuit considerations towards Spin-Based Logic
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Abstract
In this paper we review and analyze several possible implementations that could result in building logic circuits based on spintronic phenomena. We focus on majority gates driven by spintronic phenomena as they hold the promise to revolutionize circuit design. We discuss here device considerations and benchmark their performance at circuit level.

1. Introduction
Spintronic phenomena have been long studied for potential applications towards memory and logic applications. While magnetic phenomena such as giant magnetoresistance are being used in memory elements, spintronic phenomena have had little traction yet for random logic applications. This could be explained by the lack of amplification and the fact that the transistors are very efficient devices. In the larger context of Beyond CMOS devices [1], spintronic devices are being studied no longer to fully replace CMOS but to perform specific functions in the circuit and to provide new functionality.

Spintronic devices can bring non-volatility to logic circuits and in certain cases very low power operation. Spintronic phenomena are very amenable to building majority gates and several incarnations of spintronic majority gates have been proposed in the literature.

2. Majority Gates
Majority gates are multiterminal devices, which can have a large number of inputs, a large number of outputs and a set of control gates. The truth table of the simplest majority gate, with 3 inputs and one output, is presented in Table I. The state of the largest number of inputs determines the state of the output. To build universal logic, in addition to the majority gates, inverters are needed.

Table I: truth table of the simplest majority gate.

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<th>Input 1</th>
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<th>Output</th>
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The three most prominent proposals of spin based majority gates are the so called all-spin logic, spin torque majority gates (STMG) and spin wave majority gates (SWMG). All spin logic [2] uses nanomagnets with in-plane magnetization that communicate via spin coherent currents.

STMG [3] (Figure 1) uses 4 magnetic tunnel junctions (MTJs) sharing a cross-shaped free layer. The device function is based on the propagation and interaction of magnetic domain walls. Domain walls are interfaces separating regions with different magnetization direction. The conversion from the charge domain to the spin domain is done via spin transfer torque using the MTJs. The read-out of the result is done using tunnel magnetoresistance. Unlike all spin logic, STMG uses materials with magnetization perpendicular to the plane and is expected to be more energy efficient.

SWMG (Fig. 2) uses the propagation and interference of spin waves [4, 5]. Spin waves are low-energy collective excitations in magnetic materials [6]. The conversion from the charge domain to the spin domain is done using the magneto-electric elements. This conversion mechanism is expected to be most energy efficient. When benchmarking performance and discuss place and route experiments with majority gates, we will focus on these devices as they are most promising however, similar consideration apply to the STMG concept.
**STMG**

STMG devices are very interesting because the materials proposed for their fabrication are the same as those used in magnetic RAM, thus potentially allowing for same technological implementation of memory and logic devices. However, fabrication of these devices is extremely challenging as a special etch of the magnetic stacks stopping at the tunnel barrier is required for device demonstration. Also of great importance is device size, as STMG are predicted to function only for very scaled dimensions. An example of etch and patterning towards STMG device fabrication is shown in Fig. 3.

![Fig. 3: STMG. TEM cross-section of etch stopping close to the tunnel barrier interface. Insets are top-view SEM pictures of the MTJ pillars and the cross-shaped free layer. All developments are performed on 300mm wafers in the imec fab.](image)

**SWMG**

The input and output devices for SWMG are magneto-electric cells (ME) which consist of a synthetic hybrid multiferroic material. Synthetic multiferroics are stacks of piezoelectric material and a magnetostrictive material. The conduit for spin wave propagation, the spin wave bus, is a ferromagnetic material.

In Ref. [7] and [8] we have reported on benchmarking of circuits using SWMG devices and against circuits using standard CMOS. In this benchmarking we have used realistic materials parameters [9] and have accounted for the requirement to use sense amplifiers in the circuit to read the output of the SWMG. We reported there that the spin wave circuits take on average 3.5 times less area and about 400 times lower power that the equivalent circuit in CMOS. However, the spin wave circuits are on average 12 times slower. In Ref. [10] we have reported on the P&R of the SWMG using 2 primitive cells, as majority gate and an inverter. In Fig. 4 we present the metal levels for a series of large circuit benchmarks. We observe that the circuits with SWMG have a larger number of nets and higher usage of metal 4 and metal 5 layers. In is interesting to note that although the number of nets is on average 2.2 times higher for SWMG than for the CMOS design, the total wire length is about 10% lower.

![Fig. 4: Metal distribution in P&R with spin wave device cells and 10nm CMOS allowing seven metal layers.](image)

### 3. Conclusions

We have presented here a brief overview of several types of spintronic majority gates and summarized some of our work towards their experimental demonstration. We find that magnetoelectric spin wave devices could have a large power reduction compared with CMOS, however the materials required (magneto- and piezo-electric materials) are very different than current technology. Spin torque majority gates are technology friendly from a materials standpoint; however, further advances are needed to improve their performance. Majority gates in general could lead to circuit simplification [11] for certain type of applications, thus paving the way for using spintronic phenomena in logic applications.

### Acknowledgements

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### References