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Quality and Reliability Investigation of Asymmetric Low Temperature Bonding Structure Using Ultra-thin Buffer Layer Technique

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Abstract

In this research, asymmetric Cu-In/Sn bonding structure with Ni ultrathin buffer layer (UBL) was investigated. Ni UBL could defer intermetallic compound (IMC) formation between solder and Cu. Solder would tentatively maintain in liquid phase at melting point during bonding process. Therefore, this structure could reduce the solder thickness (submicron level), bonding temperature (150℃) and bonding time (15 min.). Quality and reliability tests of asymmetric structure passed and showed good results. Furthermore, asymmetric structure can separate the process of solder and electrical isolation. It is applicable for hybrid bonding process of 3D integration.

1. Introduction

Due to the microminiaturized process followed by Moore's law, critical dimension of transistor is getting smaller than before. Therefore, the size of interconnects and bumps should also be shrunk down. However, solder reduction is an issue of bump microminiaturization. Ni UBL between Cu and solder could reduce the solder thickness, slow down IMC forming during temperature rising [1], and further reduce the bonding time. In this research, we used the Ni UBL technique and In/Sn solder with low eutectic melting point (118℃) [2] to achieve low temperature Cu-In/Sn asymmetric bonding. Because of asymmetric structure, electrical isolation process and solder process should separate to avoid interaction as shown in Fig. 1.

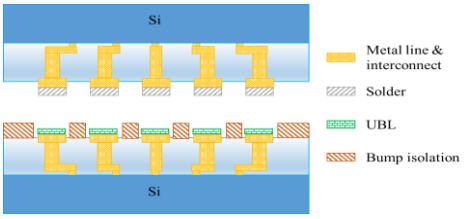

Fig. 1 The scheme of asymmetric bonding structure applied on hybrid boding of 3D integration.

2. Experimental Methods

Blanket bonding wafers and wafer-level Kelvin structures were fabricated for investigation. Metal layers were deposited onto the wafer using DC sputter and thermal coater. First, Ti and Ni adhesion layers were deposited on top and bottom 4" Si wafers by DC sputter. Next, Ni UBL was deposited after Cu layer deposition on top wafer. In/Sn solder was evaporated on bottom wafer by thermal coater. After wafer preparation, the wafers were bonded at 150℃ for 15 minute. Because of the Ni UBL, In/Sn solder would tentatively maintain in liquid phase and be flattened by bonding force. After that, IMC were formed uniformly and solidified. The metal thickness and bonding mechanism are shown in Fig.2.

The bonding quality and material analysis of bonded wafers were examined through scanning acoustic tomography (SAT), scanning electron microscope (SEM), transmission electron microscopy (TEM), energy-dispersive X-ray spectrometer (EDX) and pull test. The electrical performances were examined by temperature cycling test (TCT) and highly accelerated stress test (HAST).

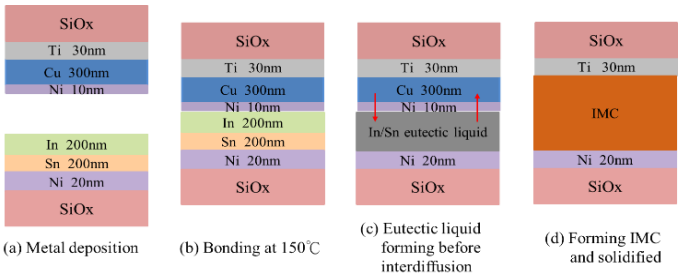

Fig. 2 The diagram of bonding structure and mechanism.

3. Results and Discussion

Bonding Quality and Material Analysis

Fig. 3 shows SAT and SEM cross-section images of bonded wafers without and with Ni UBL. Without UBL, In/Sn solder and Cu would form IMC before In/Sn melting during bonding process. IMC grain would grow and increase surface roughness and voids to lower the bonding yields and strength as seen in Fig.3 (a). By using Ni UBL, In/Sn would melt first at low temperature and increase the surface roughness tolerance. Therefore, melted solder would fill up the bonding interface before metal diffusion and rise the bonding yield as shown in fig.3 (b).

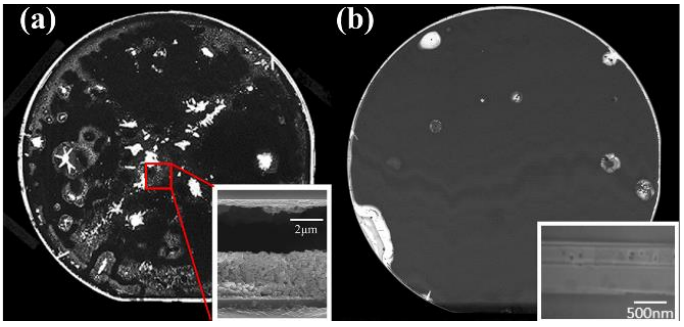

Fig. 3 SAT and SEM images (a) without and (b) with Ni UBL of bonded wafers.

TEM image and EDX result are demonstrated in Fig.4. IMC formed uniformly without voids after solder flattened. The EDX result illustrates η phase IMC forming, $Cu_2(In,Sn)$ on Cu rich side and $Cu_6(In,Sn)_5$ on solder rich side with melting point over 500℃, according to previous researches [3,4].

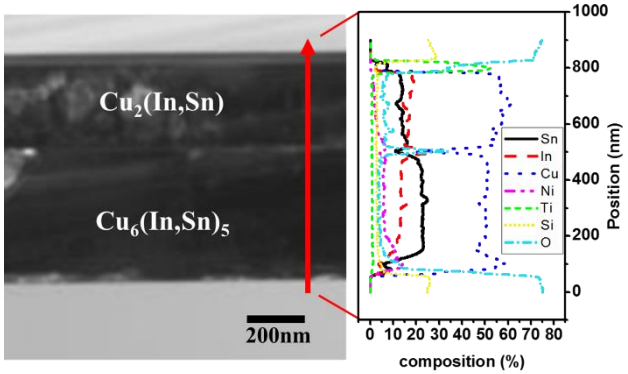

Fig. 4 TEM image and EDX analysis of uniform IMC.

Reliability of Bonding Structure

After bonding, both blanket bonded wafers and wafer-level Kelvin structure were diced into smaller pieces. Fig.5 shows the pull test diagram of one 2.25 cm^2 bonded chip. It shows good bonding strength with failure at fixture joint. Modified Kelvin structure were fabricated by lift-off process with contact area of 50x50 μ m^2 [5]. Fig. 6 shows the diagram of Kelvin structure and SAT image of wafer-level Kelvin structure that has good bonding yield. Specific contact resistances with order of 10^{-7} ohm-cm^2 are demonstrated in Fig.7 for whole wafer. Open contact was caused by surface contamination and lift-off process failure. The bonded structure is evaluated with 250 and 500 cycles TCT (JESD22-A104, -65°C to 150 °C) and un-bias HAST (JESD22A-118B, 85% RH at 130℃) for 96 hours. The results of TCT and HAST indicate Cu-In/Sn interconnect survived under large difference of temperature sweeping and high relative humidity without degradation as shown in Fig. 8. Both results illustrate a slight reduction in contact resistance because of thermal annealing during test.

4. Conclusions

Asymmetric low temperature bonding structure was successfully demonstrated by Ni UBL technique. The solder thickness and bonding time were successfully reduced. SAT, SEM and TEM images show high bonding yields. Pull test shows a high bonding strength of this structure. The specific contact resistance of the measurement is about 10^{-7} ohm-cm^2. This structure also passed TCT and HAST reliability test. All of these results show the potential of asymmetric structure that could be used for hybrid bonding of 3D integration.

Acknowledgements

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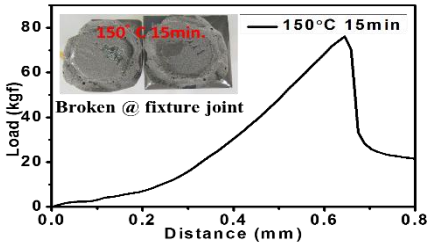

Fig. 5 Pull test results of asymmetric bonding structure.

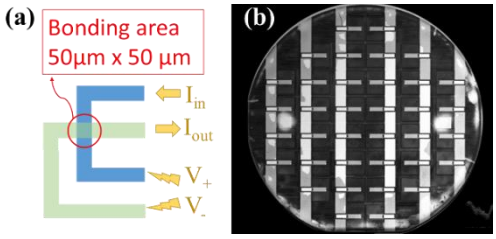

Fig. 6 (a) Modified Kelvin structure, (b) SAT image of wafer-level Kelvin structure.

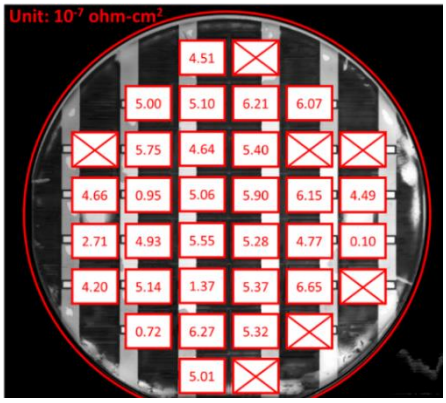

Fig. 7 Specific contact resistances of whole wafer.

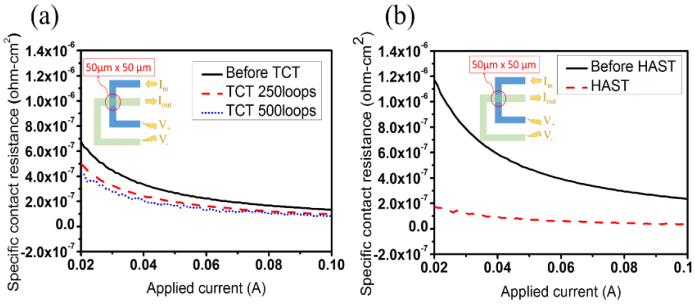

Fig. 8 Specific contact resistance of Kelvin structure (a) before and after TCT, (b) before and after HAST.

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