# Demonstration of p-Channel HfO<sub>2</sub>/GaSb MOSFETs by Using In-Situ Hydrogen Plasma Treatment

Jun-Yu Ko<sup>1</sup>, Ming-Li Tsai<sup>1</sup> and Chao-Hsin Chien<sup>1</sup>

<sup>1</sup> Development of Electronics Engineering and Institute of Electronics, National Chiao-Tung University 1001 University Road, Hsinchu 30010, Taiwan Phone: +886-3-5712121-54252 E-mail: chchien@faculty.nctu.edu.tw

#### Abstract

We employed in-situ hydrogen plasma treatment (HPT) to achieve high quality HfO<sub>2</sub>/p-GaSb interface and high performance GaSb PMOSFET. It was found that Fermi level pinning and leakage current were both effectively suppressed by HPT according to the results of capacitance-voltage (C-V) characteristics. As a result, we demonstrate a GaSb PMOSFET with a high on current of ~12 mA/mm at Vg-Vth=-2.4V and Vd=-1V, a low off current of ~1.8x10<sup>-3</sup> mA/mm at Vg-Vth = 1.1V and Vd=1V and a excellent subthreshold swing (S.S) of 236mV/dec. As compared to those in the literatures, our device depicted the highest on current and the lowest S.S. with a moderate on/off ratio.

#### 1. Introduction

GaSb has a relatively high hole mobility than silicon and most other III-V materials, which make it a potential p-channel materials in MOSFET. Nevertheless, poor high- $\kappa$ /GaSb interface results in severe fermi-level pinning (FLP) effect, which causes low modulation of capacitance and high density of interface states (D<sub>it</sub>). To improve the interface quality, insitu hydrogen plasma treatment (HPT) prior to atomic layer deposition (ALD) is a promising technique to eliminate native oxides and lower D<sub>it</sub>[1].

In this work, we demonstrated high quality HfO<sub>2</sub>/p-GaSb MOSCAPs using HPT at the start. We found that the FLP and the gate leakage current can be reduced by HPT as compared to the MOSCAPS without HPT. Finally, we make the utilization of HPT technique to fabricate PMOSFET with the developed gate stack and metal Ni alloy as source/drain.

#### 2. Experimental

(100)-oriented undoped p- and n-type GaSb substrates were used for fabricating MOSCAPs and PMOSFETs, respectively. For the fabrication of MOSCAPs, the GaSb wafers were cleaned by dilute HCl for 5 minutes to remove native oxides. Then the samples were exposed to H<sub>2</sub>/Ar mixed plasma with 200 W for 2 minutes in the ALD chamber, followed by HfO<sub>2</sub> deposition at 250 °C. Next, TiN/Al as gate electrodes was deposited by sputtering system and patterned using lift-off process. Finally, Ti/Al was sputtered on the backside of wafer as the body contact. Detailed process flow and MOSCAP structure are illustrated in the Fig. 1.

For the fabrication of MOSFETs, Ni layer was sputtered on the source/drain regions defined by lift-off technique after the aforementioned wet clean process. Then, the in-situ HPT was employed in the ALD chamber, followed by 11- nmthick HfO<sub>2</sub> deposition at 250 °C. Notably, Ni-GaSb alloy was formed simultaneously in the ALD process in order to reduce the extra thermal budget. Next, gate and contact holes were defined by photolithography and wet etching. TiN/Al metal pads were formed by lift-off process. Finally, Ti/Al was sputtered on the backside for the contact with body. Detailed process flow and device structure are illustrated in the Fig. 2.

#### 3. Results and Discussion

Figures 3 (a) and (b) show the C-V characteristics of the Al/TiN/HfO<sub>2</sub>/p-GaSb MOSCAPs without and with HPT. We can clearly observe that the modulation of capacitance was improved for the sample with HPT, indicating the FLP effect was significantly suppressed. Moreover, the gate leakage current was also tremendously decreased with HPT treatment, as shown in Fig. 4. Figs. 5 (a) and (b) shows the  $D_{it}$  distribution extracted using Berglund as well as conductance method and the Fermi level movement efficiency (FLME) profile, respectively. The  $D_{it}$  value was distributed in the range of  $10^{12}$ - $10^{14}$ eV<sup>-1</sup>cm<sup>-2</sup> and further decreased after forming gas annealing (FGA) at 250 °C for 30 minutes; this result is consistent with the improvement of FLME near the valence band edge after FGA, as shown in Fig. 5(b). In addition, the D<sub>it</sub> value was smaller near the valence band edge, implying that HPT can effectively eliminate the interface states located from the valence band edge to the mid-gap. Notice that the Dit value extracted from the Berglund method was overestimated because of limitation of CV method. To extract the D<sub>it</sub> value more accurate, the conductance method was then employed as well. The  $D_{it}$  value was of approximately  $5.1 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$  in the mid-gap. However, the likely inaccuracy by the conductance method for MOSCAPs with high D<sub>it</sub> limited the credibility of this extracted value [2]. Therefore, more accurate and convincing extraction of the D<sub>it</sub> value should be further studied.

Figs. 6 (a) and (b) exhibit the transfer and output characteristics of the p-channel GaSb MOSFET, respectively. The on/off ratio of source current higher than  $10^3$  was achieved. The subthreshold swing (S.S.) was around 236 mV/dec. Table I illustrates the comparison of key electrical parameters of our GaSb PMOSFET with those published in the literatures. Owing to the relatively high dielectric constant of HfO<sub>2</sub> (~21), the GaSb PMOSFET in this work had higher on current (~12.1 mA/mm at V<sub>g</sub>-V<sub>th</sub>=-2.4V, V<sub>d</sub>=-1V) and smaller S.S. even with thicker gate dielectric than other works.

## 4. Conclusions

In this study, we have demonstrated using HPT is able to suppress Fermi level pinning as well as leakage current and improve the interface between the dielectric and GaSb substrate. As a result, high performance GaSb PMOSFETs in terms of the highest on current and the lowest S.S. with acceptable on/off ratio were successfully fabricated as compared to the devices presented in the literatures.

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Fig. 2 (a) Process flow and (b) device structure of the PMOSFET. (c) Sectional view of the junction TEM images and (d) sectional view of the gate TEM images of the PMOSFETs.



Fig. 3 C-V characteristics of the  $Al/TiN/HfO_2/p$ -GaSb MOS-CAPs (a) without HPT and (b) with HPT.



Fig. 4 Gate leakage current of the GaSb MOSCAPs with and without HPT.



Fig. 5 (a)  $D_{it}$  distribution and (b) FLME profile of the MOS-CAPs with and without FGA.



Fig. 6 (a) Transfer characteristics and (b) output characteristics of the GaSb PMOSFETs.

Table. I Comparison of some electrical properties of GaSb PMOSFETs.

	High-k	L <sub>g</sub> (µm)	I <sub>on</sub> (mA/mm)	Ion/ Ioff	S.S. (mV/dec)
[3]	Al <sub>2</sub> O <sub>3</sub> 10 nm	5	3.0	1.5x10 <sup>4</sup>	262
[4]	Al <sub>2</sub> O <sub>3</sub> 5 nm	2	9.8	20	1427
Our work	HfO <sub>2</sub> 11 nm	2	12.1	6.9x10 <sup>3</sup>	236