Extended Abstracts of the 2016 International Conference on Solid State Devices and Materials, Tsukuba, 2016, pp559-560

N-1-06

Demonstration of a Common Gate-Stack Process for p-Ge and n-InGaAs CMOS Integration

Pei-Chia Lee[1], Cheng-Yu Chen[1], Shih-Pang Chang[2], Guang-Li Luo[2] and Jen-Inn Chyi[1,3,*]

[1] Department of Electrical Engineering, National Central University, Jhongli, Taiwan R.O.C.
[2] National Nano Device Laboratories, Hsinchu, Taiwan R.O.C.
[3] Research Center for Applied Science, Academia Sinica, Taipei, Taiwan R.O.C.
*E-mail: chyi@ee.ncu.edu.tw

Abstract

A common gate-stack process, consisting of HF cleaning, rapid thermal oxidation (RTO), and nitrogen plasma treatment, has been developed for fabricating HfO_2/Al_2O_3/(Ge, InGaAs) metal-oxide-semiconductor capacitors (MOSCAPs) with low interfacial trap density. It is observed that the RTO process produces GeO_2, InO_x and GaO_x, which may passivate Ge and InGaAs. The $GeON_x$ formed by the nitrogen plasma treatment provides a higher thermal budget for Ge MOSCAP process.

1. Introduction

High-speed low-power complementary metal-oxide-semiconductor (CMOS) logic integrated circuits consisting of Ge p-MOSFETs and InGaAs n-MOSFETs on Si substrates have been pursued extensively in recent years because of their high hole and electron mobilities, respectively. For heterogeneous integration, a common gate-stack process for both Ge p-MOSFETs and InGaAs n-MOSFETs would greatly simplify the process flow and improve the process yield. Recently, sulfur-based wet-chemical treatment and atomic layer deposition (ALD) of Al_2O_3 have been used for a common gate process. However, the residual sulfide on semiconductor surface might diffuse into gate dielectric and semiconductor after thermal process and leads to stability issues on the electrical properties. A stable and manufacturable method for surface preparation before high-κ deposition for Ge/InGaAs integration is still under development. In this work, a process, consisting of HF solution wet cleaning, rapid thermal oxidation (RTO), and nitrogen plasma treatment, is proposed for preparing Ge and InGaAs metal-oxide-semiconductor capacitors (MOSCAPs). This process is found very promising as evidenced by the low density of interface trap (D_{it}) observed on these devices.

2. Experiments

P-type Ge substrates and n-type $In_{0.53}Ga_{0.47}As$ epilayers grown on n-type InP substrates were used to fabricate the MOSCAPs studied in this work. The RTO process was conducted at 450 °C for 60 seconds in oxygen ambient. Then the samples were transferred to an ALD system equipped with a nitrogen plasma source. Prior to the deposition of high-κ material, the samples were subject to nitrogen plasma treatment for 30 sec. The dielectric deposition process was started with a 50-cycle trimethyl-aluminum treatment, then 1 nm Al_2O_3 and 4 nm HfO_2 were deposited subsequently at 250 °C. Pt/Au was evaporated on the samples as the gate electrodes through a shadow mask. A post metal annealing (PMA) process was performed at 300 °C for 10 minutes in forming gas to reduce the oxide traps and the border traps near the oxide/semiconductor interface. Capacitance-voltage (C-V) measurements were carried out at frequencies ranging from 5 kHz to 500 kHz. The D_{it} distributions within bandgap were extracted by the conductance method.

3. Results and discussion

Fig. 1(a)-(f) shows the room temperature C-V characteristics of Ge and InGaAs MOSCAPs prepared using chemical cleaning only, chemical clean+RTO, and chemical clean+RTO+nitrogen plasma processes. Using the RTO process, the interface properties of both Ge and InGaAs MOSCAPs are improved, especially for the latter, whose C-V curves display substantial increase in capacitance modulation and reduction in frequency dispersions in both the accumulation region and depletion region. The large bump at the inversion region, which is an indication of the mid-gap D_{it}, is also suppressed in the RTO treated InGaAs device. At 200 K, both the RTO treated Ge and InGaAs devices do not exhibit inversion behavior at all the measurement frequency. This implies that the traps are reduced near the Ge valence band edge and InGaAs conduction band edge. The D_{it} distribution inside bandgap, which is deduced from temperature-dependent G-V characteristics, is shown in Fig. 2. After the RTO process and nitrogen plasma treatment, the D_{it} of InGaAs MOSCAP near the conduction band edge is reduced from 7.5×10^{11} $eV^{-1}cm^{-2}$ to 3.8×10^{11} $eV^{-1}cm^{-2}$ and the D_{it} of Ge MOSCAP near the valance band edge is below 2.3×10^{11} $eV^{-1}cm^{-2}$.

To investigate the robustness of devices fabricated by this common process. The MOSCAPs are subject to annealing in nitrogen ambient at 550 °C for 10 sec. Significant degradation occurs on the Ge MOSCAPs prepared without nitrogen plasma treatment possibly because of the low thermal budget of GeO_2 interface layer (IL). While for the MOSCAP fabricated with nitrogen plasma treatment, the thermal budget is increased as shown in Fig. 3. This is accounted for by the formation of a $GeON_x$ IL. As to the InGaAs MOSCAP, no serious degradation is found by the thermal annealing.

As illustrated by the x-ray photoelectron spectroscopy spectra shown in Fig. 4, the RTO treated InGaAs surface has InO_x and GaO_x interlayers while no trace of AsO_x, which causes high D_{it}. This is consistent with earlier reports that InO_x and GaO_x play a role of passivating surface defects and dangling bonds on InAs and GaSb surfaces. $GeON_x$ is found at the interface only for the devices experienced nitrogen

plasma treatment and is believed to be reason for the increased thermal budget of Ge MOSCAP process.

3. Conclusions

In this work, we have demonstrated experimentally a common gate-stack process, which consists of an RTO process and nitrogen plasma treatment, to fabricate Ge and InGaAs MOSCAPs. As evidenced by the low D_{it} of the devices, this process is feasible for monolithic integration of n-(In,Ga)As and p-Ge channel CMOS.

Acknowledgements

This work was supported by the Ministry of Science and Technology of R.O.C. Taiwan under contract No. MOST 104-2221-E-008-035-MY3

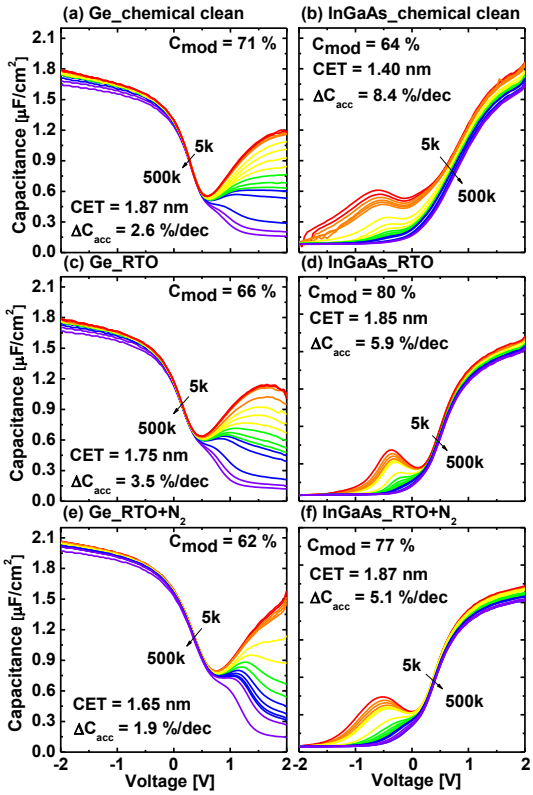

Fig. 1. Room temperature multi-frequency C-V characteristics HfO_2/Al_2O_3/(p-Ge, n-InGaAs) MOSCAPs fabricated by (a), (b) chemical clean only, (c), (d) chemical clean+ RTO, and (e), (f) chemical clean+ RTO+ nitrogen plasma treatment.

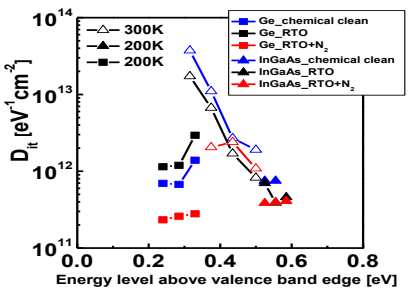

Fig. 2. Distributions of D_{it} inside the energy gap as estimated by low temperature conductance method.

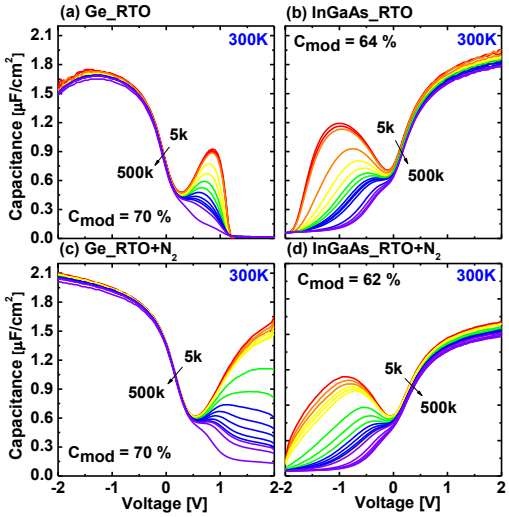

Fig. 3. Room temperature multi-frequency C-V characteristics of (a) p-Ge, (b) n-InGaAs MOSCAPs without nitrogen plasma treatment, and (c) p-Ge, (d) n-InGaAs MOSCAPs with nitrogen plasma treatment, after annealing in nitrogen ambient at 550 °C for 10 sec.

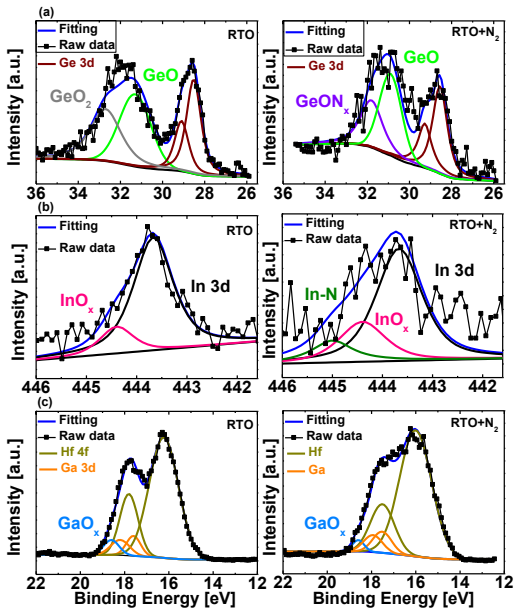

Fig. 4. Angle resolved-XPS spectra of (a) Ge 3d, (b) In 3d and (c) Ga 3d spectra of HfO_2/ Al_2O_3/ p-Ge & n-InGaAs MOSCAPs fabricated with and without nitrogen plasma treatment.