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Evaluation of Schottky Barrier Height on 4H-SiC m-face {1$\bar{1}$00} for SBD–Wall Integrated Trench MOSFET (SWITCH–MOS)

Yusuke Kobayashi[1,2], Hiroshi Ishimori[1], Akimasa Kinoshita[2], Takahito Kojima[1,2], Manabu Takei[1,2], Hiroshi Kimura[1,2] and Shinsuke Harada[1]

[1] National Institute of Advanced Industrial Science and Technology
Tsukuba Central 2, 1-1-1 Umezono, Tsukuba, Ibaraki, Japan
[2] Fuji Electric Co., Ltd.,
1-11-2 Osaki, Shinagawa-ku, Tokyo 141-0032, Japan
Phone: +81-3-6891-9600 E-mail: kobayashi-yusuk@fujielectric.com

Abstract

A 4H-SiC Schottky barrier diode (SBD)–wall integrated trench MOSFET (SWITCH–MOS) is proposed. The influence of the Schottky barrier height (SBH) on the static characteristics was simulated. A SBH of at least 0.8 eV was found to be necessary to obtain sufficient breakdown voltage. The SBH on the trench sidewall was estimated by using planar SBDs fabricated on m-face {1$\bar{1}$00} wafers with a Schottky metal of Ti or Ni. Optimal SBHs were achieved by annealing at temperatures from 400 to 700°C. The SBHs obtained for these annealing temperatures were in the range of 1.3 to 1.8 eV, which are sufficiently high for the proposed device.

1. Introduction

To reduce chip size, an integrated body–diode is preferred as the freewheeling diode in MOSFETs. However, in the case of a body–diode in a SiC MOSFET, the increase in the forward voltage owing to the bipolar forward degradation is a serious problem [1]. Furthermore, power losses by the reverse recovery current in the turn-on period and by the high forward voltage due to the high built-in potential of the p–n junction are also disadvantages of a body–diode. Therefore, an external Schottky barrier diode (SBD) connected in parallel to a MOSFET is generally utilized.

For the purpose of reducing both power loss and chip size, in this paper, we propose a 4H-SiC SBD–wall integrated trench MOSFET (SWITCH–MOS). The trench structures for the MOSFET and the SBD are expected to further reduce chip size due to cell-pitch shrinking [2–4]. Although the Schottky barrier height (SBH) is an important factor in determining device performance, the SBH on m-face {1$\bar{1}$00} as the trench sidewall has not been clarified. It is known that the SBH differs with crystallographic orientation of SiC [5–6]. We simulated the SBH dependence of the static characteristics of the proposed device, and we evaluated the SBH on the trench sidewall by fabricating a planar m-face SBD.

2. Simulation of 4H-SiC SBD–wall integrated trench MOSFET (SWITCH–MOS)

A schematic cross-section of SWITCH–MOS is shown in Figure 1. The contact trench contributes to shrinking the cell-pitch and expanding the SBD contact area. The deep p region acts as a junction barrier to shield electrical field of the Schottky barrier and the gate oxide during the off-state. In this device, the SBD is integrated on the m-face. The static characteristics of a 1.2 kV-class device were simulated with a Sentaurus Device simulator [7]. Physical parameters such as the channel mobility of the trench gate and anisotropy of the impact ionization factor were determined by fitting to the measurement results of a fabricated 4H-SiC trench MOSFET. The simulated breakdown voltage (*BV*) and the forward voltage (V_F) as a function of SBH are shown in Figure 2. When the SBH is less than 0.8 eV, the *BV* decreases due to the leakage current flowing through the SBD. On the other hand, the V_F increases linearly as the SBH increases. Figure 3 shows electron current flowing through the Schottky barrier and the hole current flowing through the p–n junction under forward bias. The current flowing through the p-n junction increases with the larger SBH because a higher bias is applied on the p-n junction. The electron current through the Schottky junction is dominant and the hole current is sufficiently small, indicating that the bipolar forward degradation is successfully suppressed in the SWITCH–MOS. An SBH of at least 0.8 eV is necessary to realize a high breakdown voltage without bipolar forward degradation.

3. Fabrication and evaluation of planar Schottky barrier diodes

We fabricated SBDs on m-face and Si-face wafers with a 1.2 kV-class drift-layer as shown in Figure 4. Ti or Ni as a Schottky metal was deposited and annealed at temperatures ranging from 400 to 700°C. The SBH as evaluated from the I–V curve is shown in Figure 5. The SBH was higher on the m-face than on the Si-face, and Ni had a higher SBH than Ti. All SBHs on the m-face were larger than 0.8 eV, indicating sufficient SBH to obtain the breakdown voltage in SWITCH–MOS. The SBH of 1.36 eV achieved with Ti and 400°C annealing was the smallest value with the lowest V_F.

4. Conclusions

The simulation study showed that an SBD–wall integrated trench MOSFET (SWITCH–MOS) realizes small cell pitch and small hole current under forward bias with an SBH of at least 0.8 eV. The optimum SBH of the SBD–wall evaluated on the m-face planar SBDs was 1.36 eV, which is sufficiently higher than 0.8 eV and small enough to suppress the bipolar forward degradation.

Acknowledgements

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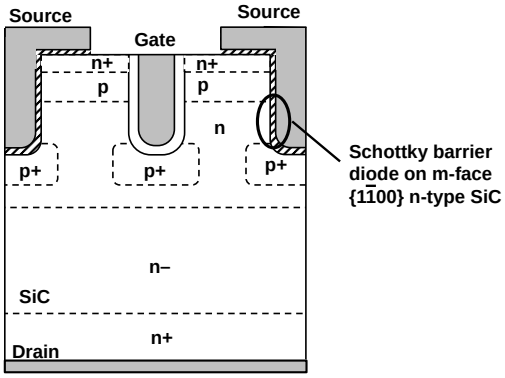

Fig. 1 Schematic cross section of the proposed 4H-SiC SBD–wall integrated trench MOSFET (SWITCH–MOS).

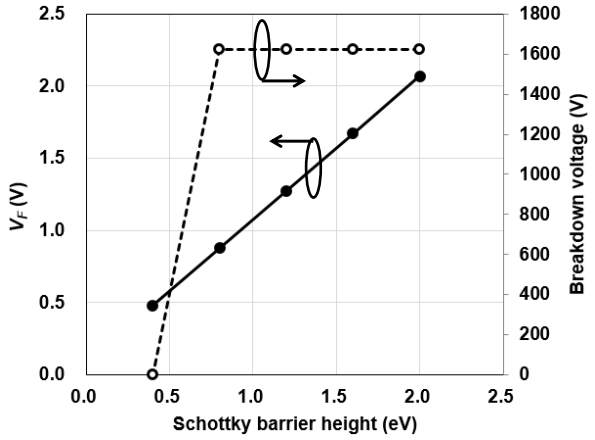

Fig. 2 Simulated forward voltage drop (V_F) and breakdown voltage (BV) depending on Schottky barrier height on the m-face of the SWITCH–MOS (Fig. 1).

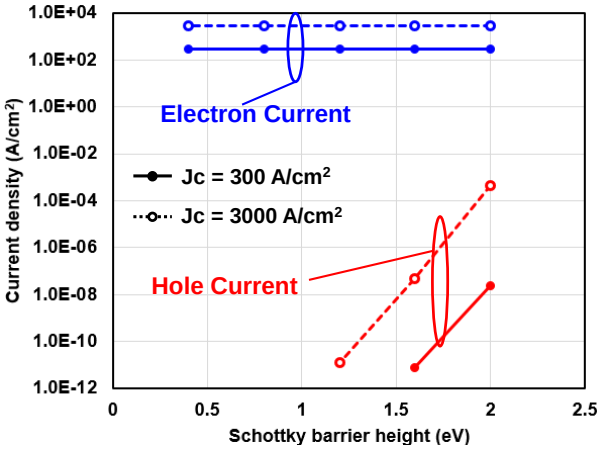

Fig. 3 Simulated electron current flowing through the Schottky barrier and hole current flowing through the p–n diode under forward bias for the SWITCH–MOS (Fig. 1).

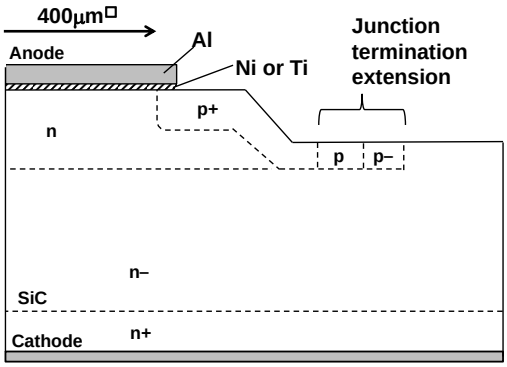

Fig. 4 Schematic cross-section of the fabricated m-face and Si-face planar Schottky barrier diode on a 1.2 kV-class drift-layer for measurement of Schottky barrier height and off-state characteristics.

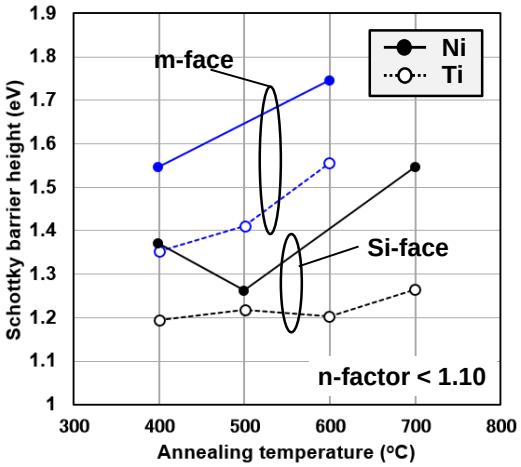

Fig. 5 Schottky barrier heights of m-face and Si-face as measured by I–V curve of a planar Schottky barrier diode (Fig. 4) depending on the kind of metal and annealing temperature.