Extended Abstracts of the 2016 International Conference on Solid State Devices and Materials, Tsukuba, 2016, pp599-600

N-6-03

High Performance Enhancement-mode Al_2O_3/AlGaN/GaN MIS-HEMT Using Standard Fluorine Ion Implantation and Partial-gate-recess

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Abstract

In this study, high performance E-mode Al_2O_3/AlGaN/GaN MIS-HEMTs fabricated by standard fluorine ion implantation and partial-gate -recess is demonstrated. The E-mode device exhibits maximum current density of 650 mA/mm, threshold voltage of 1.8 V, low on-resistance of 9.5 Ω·mm, high breakdown voltage of 860 V, low sub-threshold slope (SS) of 87 mV/decade and tiny threshold voltage hysteresis.

1. Introduction

Gallium nitride (GaN)-based high electron mobility transistor (HEMT) has been widely used in high power electronics. Due to safety-consideration, enhancement-mode (E-mode) operation is preferred for electric vehicle power device application. Several approaches have been demonstrated to achieve E-mode HEMTs in the past, such as recessed-gate, p-type GaN, and fluorine plasma implantation. Recently, owing to its simple process, E-mode device has been fabricated by combining recessed-gate and MIS (metal-insulator-gate) structure [1, 2]. However, fully recess barrier degrades channel mobility and increases channel resistance, leading to large on-resistance and low current density [3, 4]. Partial-gate-recess, remaining a thin barrier, could preserve high channel mobility but threshold voltage is not positive enough for achieving E-mode operation.

In this work, we implanted fluorine ions into both the gate insulator and the recessed-barrier layer to increase the positive threshold voltage shift for mitigating the channel damage. Fluorine ions were introduced into the GaN by ion implanter, which provides well-controlled fluorine dose and precise implantation depth. The fabricated E-mode devices exhibit high performance with a positive threshold voltage, high drain current density, high breakdown voltage, steep subthreshold slope and low threshold voltage hysteresis.

2. Device fabrication and measurement

The AlGaN/GaN HEMT structure was grown on (111) silicon substrate by MOCVD. The epitaxial structure includes a 2-nm GaN cap layer, a 25 nm $Al_{0.23}Ga_{0.77}N$ barrier layer, and a 4.3 µm buffer layer. The devices fabrication starts with ohmic contact formation of alloyed Ti/Al/Ni/Au metal stack. The planar isolation was performed by nitrogen ion implantation. To obtain clean GaN surface, in-situ nitrogen plasma treatment was performed using PECVD machine, followed by the deposition of 15-nm SiNx layer as passivation layer [5]. Nitride etch and gate recess were performed by low power ICP-RIE system. The remaining barrier thickness was about 10 nm. The 15 nm AlN/Al_2O_3 was deposited by ALD system as gate dielectric, where the AlN as interfacial layer was utilized to reduce the interface traps at Al_2O_3/GaN interface. A post–deposition annealing (PDA) was performed at 400 °C in N_2 ambient. After gate window was defined by lithography, fluorine ions were directly implanted into the gate region by Varian E500HP ion implanter. The implant energy and ion dose were 10 keV and $1x10^{12}$ cm^{-2}. Ni/Au was deposited by electron beam evaporation as the gate metal. Finally, post–metallization annealing (PMA) was carried out at 400 °C for 10 minutes in N_2 ambient to repair the implantation damages and activate the fluorine ions. A reference sample was also fabricated at same process flow but without gate recess and fluorine ion implantation for performance comparison. Agilent B1505A power device analyzer was used for DC characteristics and hysteresis measurement.

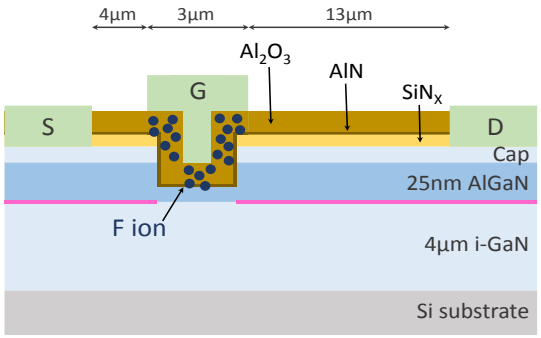

Fig. 1. The schematic cross section of the E-mode device

3.Results and discussions

The schematic cross section of the E-mode device is shown in Fig. 1. The fabricated devices feature a gate length of 3 µm, a gate-drain spacing of 13µm, gate-source spacing and gate width were 4µm and 25µm, respectively.

3.1 DC characteristics

Fig. 2(a) shows transfer characteristics of both E-mode and D-mode device. The threshold voltage, determined by linear extrapolation of the transfer curve at V_{DS} = 10 V, are -6.4 V and +1.8 V for D-mode devices and E-mode devices, respectively. Fig. 2(b) shows the transfer characteristic in the log scale of the E-mode HEMT. The steep subthreshold slope

(SS) of 87 mV/decade and the ON/OFF current ratio of ~10^{10} were obtained. Besides, very low gate leakage of 10^{-8} A/mm at V_{GS} = 9 V was observed, indicating the quality of gate insulator was preserved after fluorine ion implantation.

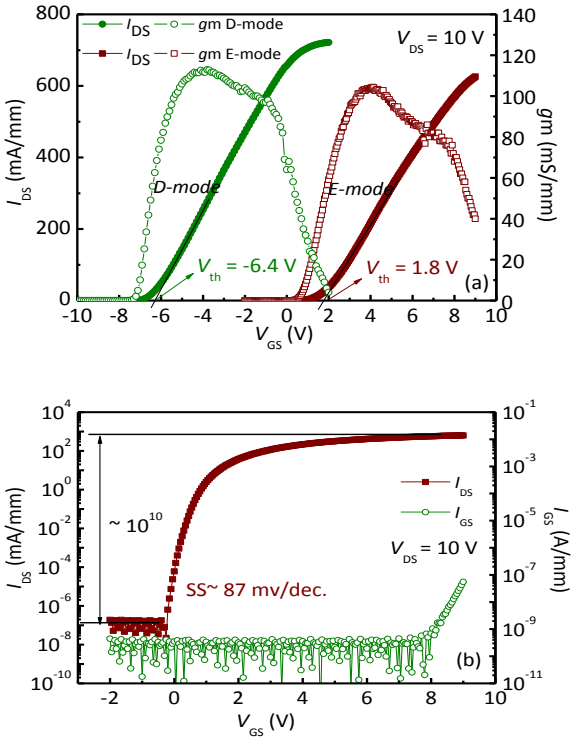

Fig. 2. Transfer characteristics of D-mode MIS-HEMTs and E-mode MIS-HEMTs in the linear scale (a) and in the log scale (b)

The output current characteristics of E-mode and D-mode devices are shown in Fig. 3. E-mode devices show the maximum current density of 650 mA/mm at V_{GS} = 9 V and the on-resistance of 9.5 Ω·mm. For comparison, D-mode devices show the maximum current density of 855 mA/mm at V_{GS} = 5 V and the on-resistance of 8.7 Ω·mm. The high drain current and the low on-resistance were obtained for E-mode device, indicating that the 10 nm AlGaN barrier remained could preserve high channel mobility and suppress the increase of the channel resistance. The breakdown voltage of E-mode device is shown in Fig. 4. The E-mode devices exhibit breakdown voltage of 860 V at drain current of 2.7 μA/mm when V_{GS} = -1 V.

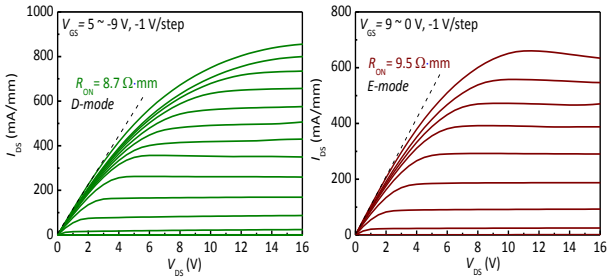

Fig. 3. I_{DS}-V_{DS} output characteristics of E-mode and D-mode MIS-HEMTs

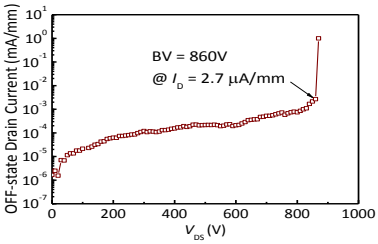

Fig.4. OFF-state drain leakage current of E-mode MIS-HEMTs

3.2 Hysteresis effect

The threshold voltage hysteresis is mainly due to the traps at the insulator/AlGaN interface. For gate-recessed GaN MIS-HEMTs, the interface traps locate more close to the GaN channel, resulting in strong electron scattering at the GaN channel, which induced threshold voltage hysteresis [6]. So, it's an important issue for gate-recessed GaN MIS-HEMTs to suppress hysteresis effect. The fabricated E-mode devices show tiny threshold voltage hysteresis (0.1 V) when the bias swept from -2 V to +9 V and +9 V to -2 V, as plotted in Fig. 5.

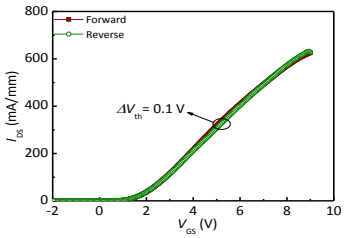

Fig. 5. I_{DS}-V_{GS} characteristics of E-mode MIS-HEMTs by up and down sweep measurements

3. Conclusions

High performance E-mode Al_2O_3/AlGaN/GaN MIS-HEMTs achieved by combining standard fluorine ion implantation and partial-gate-recess is demonstrated. The fabricated E-mode device shows a positive threshold voltage of 1.8 V, a maximum current density of 650 mA/mm, an on-resistance of 9.5 Ω·mm and an OFF-state breakdown voltage of 860 V. Compared to D-mode devices with similar process, only about 10% increase of on-resistance is observed for E-mode devices. Besides, E-mode devices also exhibited very low threshold voltage hysteresis. Thus, the proposed E-mode GaN MIS-HEMTs in this study is a promising candidate for future power electronic applications.

Acknowledgements

This work was sponsored by the TSMC, NCTU-UCB I-RiCE program, and Ministry of Science and Technology, Taiwan, under Grant No. MOST 105-2911-I-009-301 and National Chung-Shan Institute of Science & Technology, Taiwan, under Grant No. NCSIST-102-V211 (105).

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