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Normally-off operation of planar GaN MOS-HFET without using etching process

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Abstract

Normally-off operation with high drain current density was firstly demonstrated in simple planar type GaN Metal-Oxide-Semiconductor Hetero-junction-Field-Effect-Transistor (MOS-HFET) without using etching process. The obtained threshold voltage and drain current density were +3.0 V and 0.4 A/mm, respectively.

1. Introduction

Field-effect transistors using a hetero-junction of GaN related wide band-gap semiconductor materials are now applying not only to high-power RF devices [1] but also high-power switching devices [2] due to its high electron mobility and high electric breakdown field. In the case of applying to high-power switching devices, a normally-off operation is specially required for safety. Some transistor structures for the normally-off operation have been proposed recently. One of them is AlGaN/GaN high-electron-mobility-transistors (HEMTs) with recessed Metal-Insulator-Semiconductor gate structures.[3-4] In these structures, etching process is needed to form the recess gate structure. Another candidate is Gate-Injection-Transistor structure using a p-type GaN layer under a gate electrode.[5] In this structure, etching process is also needed to remove the p-type layer at the outside of gate region. However, an etching process in GaN related semiconductors were very difficult due to its large binding energy. This difficulty of etching process causes an insufficient uniformity in threshold voltage and drain current density.

In this study, we propose simple planar type GaN MOS-HFETs without using the etching process. In this structure, a Si ion implantation technique was employed to form ohmic contact region and access region between ohmic electrodes and channel region. A barrier layer was designed not to generate two-dimensional electron gas (2DEG) at hetero-interface, and Al_2O_3 film, which was deposited by plasma enhanced atomic layer deposition, was applied as a gate oxide layer.

2. Experimental

Figure 1 shows a cross-sectional structure of fabricated GaN MOS-HFETs. An AlN/GaN hetero-junction was employed in order to use high mobility electrons as carriers in channel region.[6] A thickness of an AlN barrier layer was set not to generate 2DEG at a hetero-interface in zero bias condition. These layers were grown on a Simi-Insulated (SI) SiC substrate by metalorganic chemical vapor deposition technique. A measured sheet resistance of the epitaxial layer was over $1x10^5$ Ω/sq.

Fabrication process of MOS-HFETs started with a formation of ohmic contact region and access region between ohmic electrodes and channel region under gate electrodes. These regions were formed by a Si-ion implantation technique and a subsequence high temperature activation annealing by Rapid-Thermal-Annealing technique. Source and drain ohmic electrodes were formed on these Si ion implanted region. Then device isolations were performed by using ion implantation technique. Next, Al_2O_3 gate oxide layer was deposited by plasma enhanced atomic layer deposition. A thickness of Al_2O_3 was set to 30 nm. Finally, gate electrodes, which covered all of channel region between Si ion implanted regions, were formed. DC characteristics measurements were performed using finger type FETs with a channel length of 1 μm and a width of 100 μm.

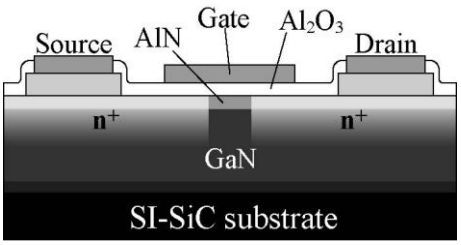

Fig.1 Schematic cross-sectional structure of fabricated planer type GaN MOS-HFET.

3. Results and discussion

First, characteristics of Si ion implanted regions and ohmic contacts were evaluated by using a transfer length method. A obtained sheet resistance, a contact resistance and a specific contact resistance were 210 Ω/sq, $8x10^{-6}$ Ωcm^2 and 0.4 Ωmm, respectively. It was confirmed that Si ion implantation technique was effective to from the low resistive ohmic contacts and access region.

Figure 2 shows a gate voltage (V_g) dependence of a drain current density and a transconductance in the fabricated GaN MOS-HFETs with the channel length of 1.0 μm. These were measured at a drain voltage of 5 V. In the

fabricated GaN MOS-HFET, we confirmed a normally-off operation with sufficiently high threshold voltage (V_{th}) of +3.0 V. An obtained maximum drain current density was also sufficiently high of 0.4 A/mm. An obtained maximum transconductance was 91 mS/mm, and an intrinsic transconductance was calculated from the obtained maximum transconductance, a contact resistance and a sheet resistance. The calculated intrinsic transconductance was 0.10 S/mm. We also calculated an electron saturation velocity (v_s) using the intrinsic transconductance, and it was 4.1 x 10^6 cm/s. In this calculation, dielectric constants of AlN and Al_2O_3 were set to 8.5. This calculated electron saturation velocity was almost same value to the one of conventional normally-on GaN-HEMTs.[7] Therefore these results indicate that this simple planer transistor structure without using etching processes has a potential to become one of candidates for high-power switching devices.

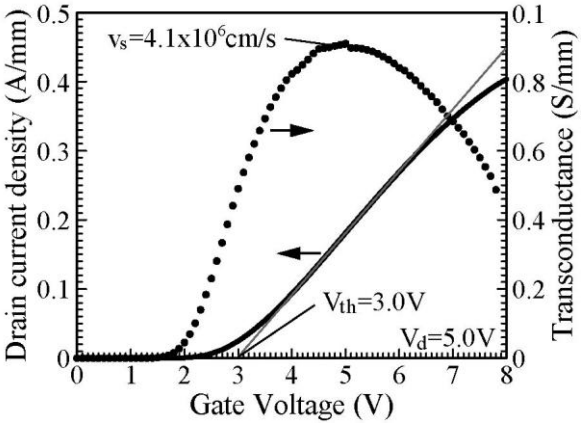

Fig.2 Gate voltage dependences of drain current density and the transconductance at a drain voltage of +5V in fabricated GaN MOS-HFET with the channel length of 1μm.

Figure 3 also shows a gate voltage dependence of a drain current density with semi-logarithmic scales in the fabricated GaN MOS-HFET with the channel length of 1.0 μm. The drain current increase over gate voltage of 0 V, and complete normally-off operation was demonstrated. An obtained subthreshold swing (S.S.) was 176 mV/dec.

Figure 4 shows drain current-drain voltage curves in the fabricated GaN MOS-HFET with the channel length of 1.0 μm. In this graph, we could also confirm the clear normally-off operation with sufficiently high drain current density of 0.4 A/mm.

4. Conclusions

We proposed simple planar type GaN MOS-HFETs without using the etching process to realize a normally-off operation for high-power switching devices. In fabricated GaN MOS-HFETs, complete normally-off operation was demonstrated. The obtained threshold voltage and maximum drain current density were sufficiently high of +3.0 V and 0.4 A/mm, respectively. The calculated electron saturation velocity from measured transconductance was also sufficiently high of 4.1 x 10^6 cm/s. These results indicate that this simple planer transistor structure without using etching processes has a potential to become one of candidates for high-power switching devices.

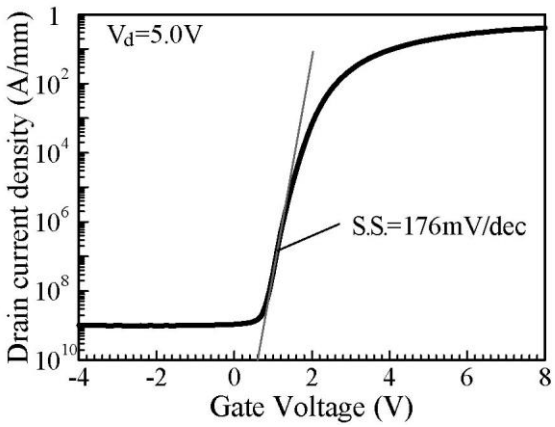

Fig.3 Gate voltage dependences of drain current density with semi-logarithmic scale at a drain voltage of +5V in fabricated GaN MOS-HFET with the channel length of 1μm.

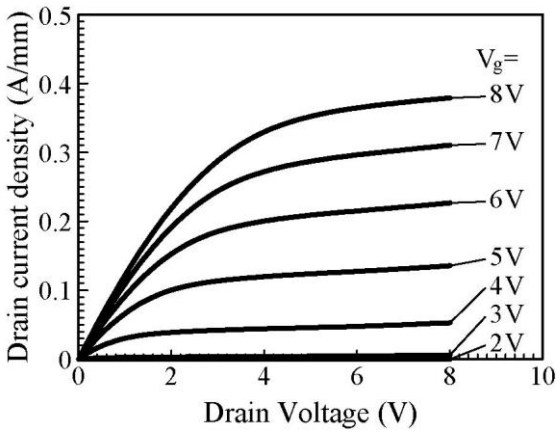

Fig.4 Drain current-drain voltage curves in fabricated GaN MOS-HFET with the channel length of 1μm.

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