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Si-passivated Ge nFET towards a reliable Ge CMOS

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Abstract

This paper shows Si-passivated Ge nFETs with high electron mobility and superior PBTI reliability, demonstrated on a 300 mm Si wafer platform. While the optimization of Si thickness improves the electron mobility, band engineering using La-induced interface dipole and defect passivation using laser annealing improves the PBTI reliability. This highlights the advantage of using Si-passivation layers.

1. Introduction

Germanium has the potential to replace the Si channel in the future CMOS thanks to its high electron and hole mobility. For pFET, the passivation of the Ge surface using a thin Si layer is quite efficient since a sufficient band offset between the valence band E_v of Si and Ge confines the holes in the Ge channel. High hole mobility of strained Ge pFET outperforming Si pFET has been demonstrated using the Si cap layer (Fig. 1) [1]. Note that NBTI reliability can also be improved by using a Si cap on Ge pFET thanks to 1) the energy decoupling between the holes at the E_v of Ge and the defects in the high-k/SiO_2, and 2) the use of a SiO_2 interlayer (IL) instead of GeOx which contains a high density of hole trapping sites (Fig. 2) [2]. For Ge nFET, on the other hand, significant improvement in electron mobility has been demonstrated by using GeOx based gate stacks which provide low D_{it} and high mobility [3]. However, the PBTI reliability of such gate stacks is a serious concern and has been reported only recently [2, 4]. Here, the Si cap route has also shown the potential to improve the PBTI reliability of Ge nFET [5]. The use of a SiO_2 IL enables interface dipole engineering at the high-k/SiO_2 interface, which has been a V_T tuning technique on Si [6]. Furthermore, both a common channel and common gate stack solution for n/pMOS will be beneficial in terms of process simplicity and cost effectiveness. Thus, we have focused on Ge nFET with Si passivation. The concerns about using Si cap are the high D_{it} [3] and/or the possible electron transport in the Si layer, both of which result in low electron mobility. While the former issue needs to be addressed by some process improvement, the latter issue is expected to be mitigated by reducing the Si thickness down to a few monolayers where quantization is expected to increase the conduction band E_c of the Si and release the electrons from the Si layer [7] (Fig. 3). Since the physical thickness of the Si is also limited, electrons are expected to be distributed in the Ge channel.

2. Device fabrication

Figure 4 summarizes the process flow of the Si-passivated Ge gate stack as well as that of the GeO_x based stack as a reference. The key processes are 1) the epitaxial Si growth on Ge with Si_3H_8 precursor at 350°C followed by dry O_3 oxidation, 2) the PVD La deposition at different gate stack position, and 3) laser annealing at 750°C after HfO_2 deposition.

3. Impact of Si cap thickness on mobility and PBTI reliability

The presence of the Si cap is electrically detected by the increase in T_{inv} of the pFET (Fig. 5). The abrupt increase in T_{inv} for the grown Si thinner than 0.8 nm is attributed to the formation of GeO_x under the fully oxidized Si layer. The electron mobility shows a significant increase by using a thin Si layer, outperforming the GeO_x-based gate stack (Fig. 6). The optimum initial Si thickness in terms of the electron mobility is found to be 0.9 nm for the used oxidation process. The PBTI reliability also shows a strong impact of the Si thickness. While a maximum V_{ov}/T_{inv} of 3.8 MV/cm is achieved with the 2.0-nm-thick grown Si, it degrades as the Si thickness is reduced. This trade-off between mobility and PBTI reliability is interpreted as follows (Fig. 7): for the thin Si cap layer, the mobility is enhanced by both improved the interface properties, and by the spillover of electrons into the Ge channel layer; however, the shallower effective E_C favors electron trapping in the HfO_2 defect levels as sketched out in Fig. 7 and degrades the PBTI reliability [2]. To overcome the trade-off, while the Si thickness is kept constant to provide the high electron mobility, La is introduced to create an interface dipole at HfO_2/SiO_2 interface, which is expected to increase the energy misalignment between the electrons and the defects in the HfO_2 by shifting the band diagram of HfO_2 (Fig. 7 (c)).

4. Band engineering using La-dipole for PBTI reduction

The amount of La at the HfO_2/SiO_2 interface is optimized on MOSCAPs (Fig. 8). A significant and abrupt negative V_{fb} shift is seen only when La is deposited on SiO_2, indicating the effect of La-induced interface dipole. CET reduction is seen only when the right amount of La is deposited on SiO_2 thanks to the LaSiO formation having a higher k-value than SiO_2 (Fig.8). While similar trends are confirmed on MOSFETs, the laser annealing shows further reductions in V_{th} and T_{inv}, resulting in an EOT of 0.95 nm. The high electron mobility of the optimized Si cap (~175 cm^2/Vs) is maintained after La incorporation and laser annealing at $N_s=5\times10^{12}$ cm^{-2}, with even an increased peak mobility (240 cm^2/Vs) at thinner T_{inv} (Fig. 9). The PBTI reliability is improved by adding La (Fig. 10). The confirmed increase in slope (γ/n, where γ is the voltage acceleration factor and n is the time exponent) indicates the misalignment of the carriers to the defects in the high-k (Figs. 10 and 7(c)) [4]. Further improvement is obtained by laser anneal, however, no increase in slope is found, indicating that the overall defect density is reduced rather than further energy decoupling between the carriers and defects in the gate dielectrics. Moreover, the laser annealing causes no change in PBTI reliability when there is no La. This suggests that the additional improvement in PBTI reliability thanks to the laser annealing is related to defect passivation in the LaSiO layer. The achieved maximum V_{ov}/T_{inv} is 1.9 MV/cm, coming from the V_{ov} of 0.28 V and the T_{inv} of 1.5 nm, which is the best reliability for Ge nFET with a high electron mobility to the best of our knowledge. The improvement on electron mobility and PBTI reliability of Ge nFET is summarized in Fig.11.

5. Conclusion

We have demonstrated a well-balanced Ge nFET with respect to performance and reliability by using an ultrathin Si passivation layer combined with La-cap and laser annealing. Band engineering focusing on quantization in the Si passivation layer and interface dipole formation are key enablers.

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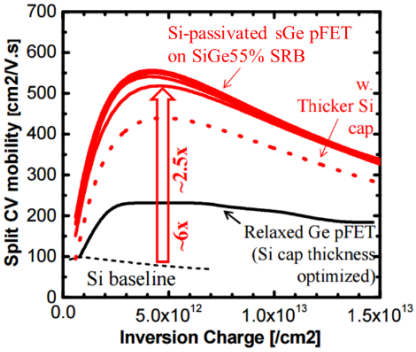

Fig.1 High hole mobility of strained Ge pFET demonstrated by using Si-passivation layer [1].

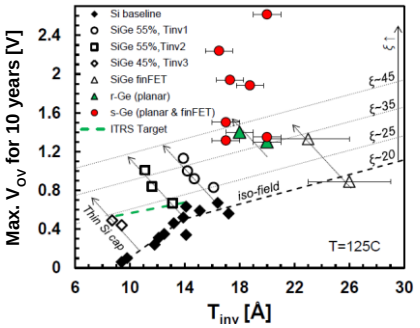

Fig.2 Superior NBTI reliability of strained Ge pFET on SiGe strain relaxed buffer. ξ represents energy decoupling between carriers and defects [2].

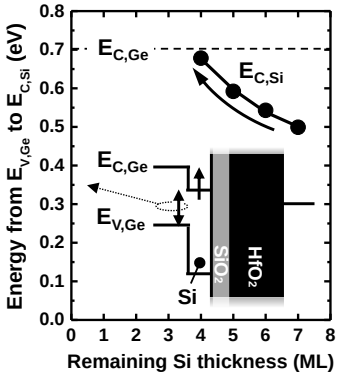

Fig.3 Simulated energy difference between E_C of Si and E_V of Ge [7]. The Effective E_C of Si cap is expected to increase while reducing Si thickness thanks to quantization.

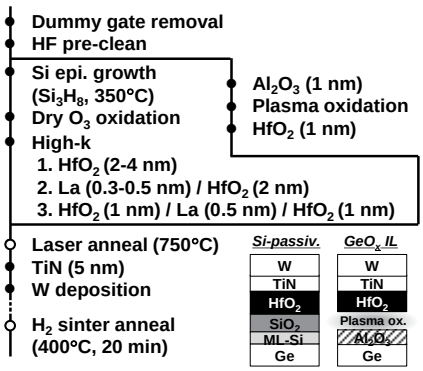

Fig.4 Fabrication process of gate stacks with Si passivation layer and GeO_x IL.

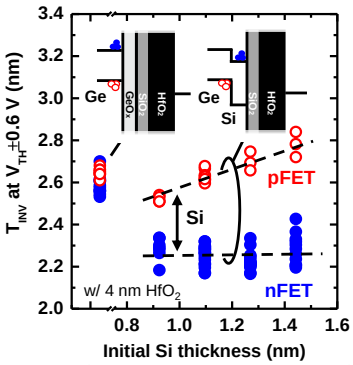

Fig.5 T_{INV} of p/nFET extracted at V_{th}±0.6 V as function of initial Si thickness. T_{INV} of pFET changes with Si thickness while that of nFET stays constant. The too thin Si thickness <0.8 nm causes GeOx formation and increase Tinv of both n/pFETs.

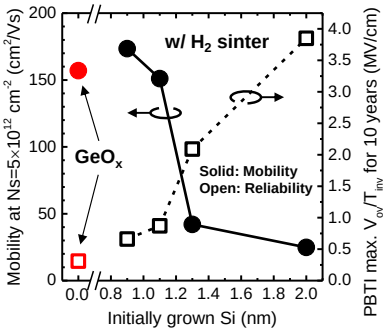

Fig.6 Si cap thickness-dependent trade-off between electron mobility and PBTI reliability on Ge nFETs. Electron mobility of Ge nFET with optimized Si thickness is higher than that of nFET with GeO_x based gate stack.

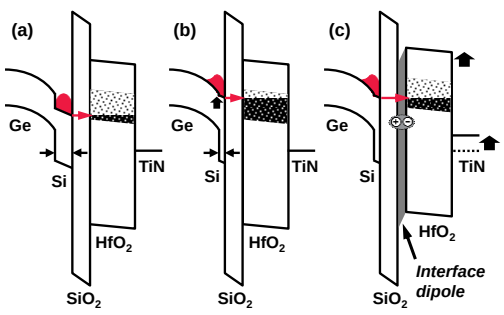

Fig.7 Band diagrams of Si-passivated Ge nFETs with (a) thick Si layer, (b) thin Si layer and (c) thin Si layer with interface dipole at high-k/SiO_2 interface.

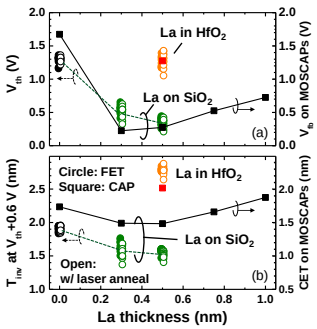

Fig.8 (a) V_{th} and V_{fb}, (b) T_{inv} and CET of La-incorporated Si-passivated gate stack. La deposition on SiO_2 causes V_{fb} and CET reduction while the excess of La increases V_{fb} due to the additional negative charges and CET.

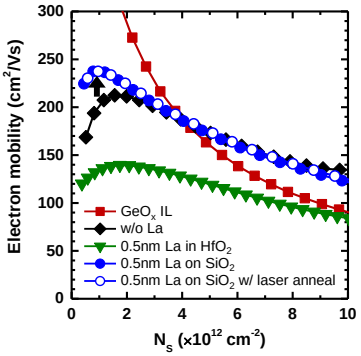

Fig.9 Electron mobility vs N_S for the La-incorporated Si-passivated Ge nFETs.

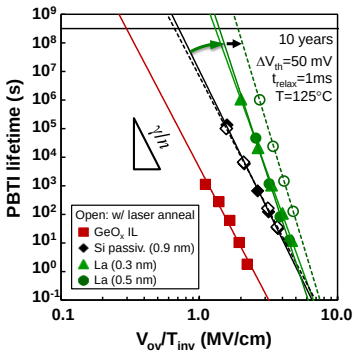

Fig.10 PBTI lifetime vs. V_{ov}/T_{inv} showing the improved PBTI reliability by La-cap on SiO_2 and laser anneal. γ/n is an indicator of the defect misalignment between carriers and defects in gate stack.

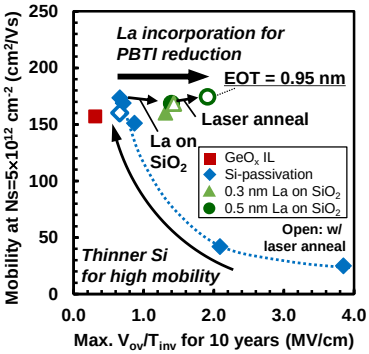

Fig.11 Trade-off between electron mobility and PBTI reliability of Si-passivated Ge nFET and improvement by La incorporation.