**Thickness-Defined Poly-Si FinFETs (TD-FinFFTs) with 5nm Fin-Width and Performance Enhancement by Local Strain Boost Technique**

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**Abstract**

This paper demonstrates the novel Thickness-Defined FinFETs (TD-FinFFTs) with extreme-narrow fin width of 5nm by means of Low Temperature-Atomically Level Etching (LT-ALE). The quantum-sealed fin-width of TD-FinFFTs contributes not only the excellent electrical characteristics, but also transconductance improvement. The fabricated TD-FinFFTs has a good subthreshold swing (S.S.) of 115 mV/dec., small drain-induced barrier lowering (DIBL) of 30mV/V and high \( I_{on}/I_{off} \) ratio (\( 1\times10^8 \)). The on current enhanced by the reduction of surface roughness scattering (SRS) and local strain booster technique. TD-FinFFTs provides the feasibility for the application of three-dimensional high-density integrated thin-film devices with economical fabrication.

1. **Introduction**

In order to increase the number of transistors in unit area of integrated circuit, scaling down of the IC devices or 3D-vertically stacked circuits are urgent studies. Over the past few years, the monolithic 3D-ICs with poly-Si channel has been successfully demonstrated [1] and the performance improved by multi-gate configuration and fully-depleted channel [2]. Although the fin channel can easily formed by spacer image transfer (SIT) scheme with improved line edge roughness (LER) [3], the dry-etching process induced damage at Si sidewall will decrease the mobility due to the increased roughness and contamination [4-5]. The motivations of this paper are (1) to minimize the dry etching effect (2) to provide an alternative route by an economical litho-process for extreme-narrow fin-width fabrication (3) to maintain the dense fin pitch by the vertical stacked scheme and (4) to enhance the performance by local strain technique.

2. **Experiment**

The 3D cross-sectional view and key process steps of the TD-FinFET are shown in Fig. 1 and Fig. 2. The Si wafer with 500nm SiO2 was served as starting wafer. First, the wet etching stop nitride, bottom TEOS oxide and un-doped amorphous-Si layers were then deposited by LPCVD with the thickness of 15/45/10nm, respectively. The a-Si layer was then thinned by 75°C low temperature-atomic level wet etching (LT-ALE) featuring a slow etching rate (0.7nm/min) which can offer a good etching uniformity. This technique can utilize to define the uniform fin width within one wafer. Then, a 100nm TEOS oxide was deposited for top isolation layer. After nanobelt region was patterned, some wafers were annealed by RTA at 1000°C for 10 sec. in N2 ambient. This step provide the strain to the channel and memorized the stress. Then, n-type in-situ doped a-Si was deposited for raised S/D and crystallized by conventional SPC. After raised S/D pad defined by RIE. Dilute HF solution (1:100) was used to laterally etch and then exposed the poly-Si fins as well as controlling the fin height at this step. In this work, the different aspect ratio (AR=\( H_{fin}/W_{fin} \)) of fins were fabricated. After channel fin formation, the TEOS gate oxide and in-situ n+ poly-Si with were deposited and etched to form the gate electrode.

3. **Result and discussion**

The TEM image of one layered TD-FinFET is shown in Fig. 3. The AFM inspection with the same thinning process of a-Si layer are shown in Fig. 4. After LT-ALE process, the surface roughness is nearly same with initial morphology of a-Si. The \( I_{on}-V_{DS} \) with different number of fins (\( N_{fin} \)) are shown in Fig. 5. \( I_{on} \) increased as the \( N_{fin} \) increased and the \( I_{off} \) can be maintained below \( 1\times10^{-12} \)A. Fig. 6 shows the comparison of different nanobelt width fabricated in same wafer with identical AR of fins. There has no drain current difference between different nanobelt widths. The conduction current generated in the exposed fins and controlled by the gate. The impact of AR shows in Fig. 7, the poor S.S. in short-fin may ascribe to the dry etch damage during nanobelt region formation. The dry etching damage the sidewall of 5nm nanobelt (i.e. top area of the fin channel) and the (fin-width/effective width, \( W_{fin}/W_{eff} \)) ratio is larger in short-fin device, where the \( W_{eff} \) is count as (\( W_{fin} \times H_{fin}/2 \)). Thus, the short-fin suffers more defects in the conduction current path and consequently degrade the switching behavior. This problem can solved by taller-fin with smaller (\( W_{fin}/W_{eff} \)) ratio. Fig. 8 shows the performance enhancement on tall-fin, the \( g_m \) and \( I_{on} \) has significant improvement by the local strain boost technique. The \( g_m \) versus \( V_{DS} \) displays the immunity of surface roughness scattering owing to the quantization benefit. Fig. 9 shows the \( I_{on}-V_{DS} \) with and without strain. Because the fin channels can effectively controlled by the gate, both of them has kink-effect free characteristic.

4. **Conclusion**

The novel TD-FinFET with 5nm fin width was successful fabricated and characterized by a very simple method with the assistance of LT-ALE. The method has a highly potential for vertical stacking of multiple fin channels. The performance of TD-FinFET enhanced by quantization effect and local strain boost technique. The purpose TD-FinFET show the great potential for 3D-ICs application.
Fig. 1. (a) 3D cross-sectional view of the TD-FinFET with one-layered fin channel.

Fig. 2. (a) Key fabrication steps of TD-FinFETs (b) cross-section flow at the specific area correspond to fig. 1.

Fig. 3. TEM images of TD-FinFET (a) one Si layer and one strip region contribute two fins (b) enlarged image of fin dimension ($W_{fin}=5\text{nm}$, $H_{fin}=18\text{nm}$, gate oxide=4nm) (c) enlarged image of poly-Si fin channel and (d) schematic diagram of purposed TD-FinFETs with vertical-stacked multi-fins along the gate direction.

Fig. 4. AFM images of (a) as deposited un-doped a-Si film and (b) after LT-ALE thinning process.

Fig. 5. $I_D-V_G$ of TD-FinFETs with different number of fin channels.

Fig. 6. $I_D-V_G$ of TD-FinFETs with different nanobelt width ($W_{NB}$).

Fig. 7. $I_D-V_G$ of TD-FinFETs with different AR of fin channel. S.S. degrade in short-fin.

Fig. 8. $I_D-V_G$ and $g_m$-$V_G$ characteristics. Performance enhanced by local strain boost technique.

Fig. 9. $I_D-V_D$ characteristics of TD-FinFETs. The strained device present the significant enhancement of drive current.

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References