Demonstration of Ultra-Thin Buried Oxide Germanium-on-Insulator MOSFETs by Direct Wafer Bonding and Polishing Techniques

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1. Introduction
Germanium is considered as a promising channel material for future CMOS technology, due to its higher mobility than Si. To adopt Ge channels to the current CMOS technology, the Germanium-on-Insulator (GeOI) structure has attracted great attention due to its advantages in electrostatic controllability of MOSFETs [1, 2]. In order to fully utilize the benefits of GeOI MOSFETs, it is mandatory to realize the fully depleted GeOI channel, as well as the formation of ultra-thin buried oxide is also necessary for the modulation of carrier transport in GeOI channels [3, 4]. Several methods have been proposed to fabricate GeOI substrates, such as Smart Cut™ [5], Ge condensation [6] and liquid epitaxy [7]. However, the crystal qualities of Ge layers in these GeOI structures, especially ultra-thin body and ultra-thin buried-oxide (UTBB) GeOI structures, are still not sufficiently high to realize GeOI MOSFETs with superior electrical properties. Thus, UTBB GeOI substrates with superior Ge qualities are the key to fabricate high performance Ge transistors for future CMOS technologies. In this study, the direct wafer bonding and polishing techniques have been employed to realize the UTBB GeOI structures which preserve the crystal quality of the ultra-thin Ge layer similar to bulk Ge. The GeOI nMOSFETs have also been fabricated with these GeOI structures, which further confirm the high crystal quality of the UTBB GeOI structures.

2. Experimental
The fabrication process of UTBB GeOI structures is shown in Fig. 1. After pre-cleaning of the Ge donor wafers (2×10¹⁶ cm⁻³) and the Si handle wafers, the 6.5-nm-thick Al₂O₃ layers were deposited by ALD. The wafer bonding was carried out to fabricate the Ge/Al₂O₃ (13 nm)/Si structure. The bonded wafer was annealed at 300 °C for 1 hour in N₂ ambient. The mechanical polishing and the CMP was conducted to decrease the Ge layer thickness and reduce the surface roughness of Ge. Followed by the Hall bar mesa etching, the metal electrodes were formed as the contact pads for Hall bar devices and S/D for GeOI nMOSFETs.

3. Results and Discussion
The cross section TEM (Fig. 2) confirms that the UTBB GeOI structure with a minimum Ge thickness of 9 nm and ultra-thin BOX of 13 nm has been realized. As shown in Fig. 3, the GeOI structure exhibits a small surface roughness with the RMS around 0.2 nm, which is comparable with that of the original Ge donor substrate (RMS=0.2 nm). The Ge layers in UTBB GeOI structure maintain the crystal quality originated from the bulk Ge, indicated by the strong peak intensity and the small widening of the peak in the XRD spectrum (Fig. 4). This phenomenon is also confirmed from the same Raman peak width of GeOI structures with different Ge thicknesses of 60 and 20 nm, with that of the bulk Ge (Fig. 5). A slight red-shift of the Raman peak compared to the bulk Ge is also observed in Fig. 5, indicating a little tensile strain of 0.1% was introduced. This phenomenon is attributable to the difference of the thermal expansion coefficient between Si and Ge. Fig. 6 shows the electron and hole mobility as a function of GeOI thickness, with the comparison to the reference bulk Ge data. For the p-GeOI, the hole mobility of 1330 cm²/Vs is achieved under a Ge thickness of 537 nm, which agrees well with the hole mobility in the bulk Ge with doping concentration of 2×10¹⁶ cm⁻³. With a decrease of the Ge layer thickness, the reduction of Hall mobility is observed GeOI structures. The hole and electron mobilities are plotted as a function of carrier concentration (Fig. 7). It is found that the Hall hole mobility in p-GeOI is slightly lower than that in bulk Ge even if the GeOI thickness is aggressively reduced, meaning that the crystal quality originated from bulk Ge has been almost maintained. For n-GeOI, the stronger degradation of Hall electron mobility is observed during the thinning of Ge layer, which is attributable to the fact that the electron mobility in Ge is more sensitive to defects than hole.

The back-gated UTBB GeOI nMOSFETs with the inversion operation mode have been fabricated. Fig. 8 show the Iₛ-Iᵥ and Iₛ-Iᵥ characteristics of the GeOI nMOSFETs with a Ge thickness of 64 nm, respectively. It is found that the impact of GeOI thickness on the Iₛ-Iᵥ characteristics and electron mobility is relatively weak (Fig. 9). However, it is noted that the mobility in these GeOI nMOSFETs are still not sufficiently high, and this could be due to the poor interfacial quality of Ge/Al₂O₃ since the interface has not been optimized yet. The high field mobility (190 cm²/Vs at Nₛ=1×10¹⁷ cm⁻³) of the GeOI nMOSFET is similar with that in the unoptimized bulk Ge nMOSFETs with the same Al₂O₃/Ge interface [8]. Thus, the improvement of the electron mobility in these GeOI nMOSFETs is expectable with further reduction of Dₛ at the MOS interface.

4. Conclusions
The high quality UTBB GeOI structures have been fabricated through utilizing bulk Ge as the donor wafer by wafer bonding and polishing techniques. The ultra-thin Ge body of 9 nm and the ultra-thin BOX of 13 nm have been realized simultaneously, which still maintain the superior crystal quality originated from bulk Ge. These results indicate the feasibility of direct wafer bonding and polishing techniques in future CMOS technology.

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Figure 1: GeOI fabrication flow by wafer bonding and thinning process.

Figure 3: AFM result of the UTBB GeOI.

Figure 4: The XRD spectrum of a GeOI structure with Ge thickness.

Figure 5: The Raman spectra with different Ge thicknesses, compared with bulk Ge.

Figure 6: The Hall mobilities taken from the UTBB GeOI structures with different Ge layer thicknesses.

Figure 7: The Hall mobilities in the UTBB GeOI structures, plotted as functions of carrier concentration.

Figure 8 (a), (b): $I_d$-$V_d$ and $I_d$-$V_g$ curves of the back-gate GeOI nMOSFETs with Ge thickness of 64 nm. The dimensions of these devices are $W/L=100\mu m/400\mu m$.

Figure 9 (a), (b): $I_d$-$V_g$ curves and effective electron mobility of the back-gated GeOI nMOSFETs with different Ge thicknesses.