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Crossbar arrays for Storage Class Memory and non-Von Neumann computing

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Abstract

I discuss recent work towards large crossbar arrays of NVM for Storage Class Memory and non-Von Neumann computing, incorporating advancements in nonlinear Access Devices and in the understanding of how device imperfections can adversely affect neural network performance.

1. Introduction

For more than 50 years, the capabilities of Von Neumann-style information processing systems — in which a "memory" delivers operations and then operands to a dedicated "central processing unit" — have improved dramatically. While it may seem that this remarkable history was driven by ever-increasing density (Moore's Law), the actual driver was Dennard's Law: a device-scaling methodology which allowed each generation of smaller transistors to actually perform better, in every way, than the previous generation.

Unfortunately, Dennard's Law terminated some years ago, and as a result, Moore's Law is now slowing considerably. In a search for ways to continue to improve computing systems, the attention of the IT industry has turned to Non-Von Neumann algorithms, and in particular, to computing architectures motivated by the human brain.

2. Storage Class Memory

At the same time, memory technology has been going through a period of rapid change, as new nonvolatile memories (NVM) — such as Phase Change Memory (PCM), Resistance RAM (RRAM), and Spin-Torque-Transfer Magnetic RAM (STT-MRAM) — emerge that complement and augment the traditional triad of SRAM, DRAM, and Flash. While these NVM candidate technologies are still relatively unproven compared to Flash, there is a strong opportunity for one or more of them to find success in applications that do not involve simply "replacing" NAND Flash.

Such memories could enable Storage-Class Memory (SCM, Figure 1) — an emerging memory category that seeks to combine the high performance and robustness of solid-state memory with the long-term retention and low cost of conventional hard-disk magnetic storage. Storage Class Memory creates two entirely new and distinct levels within the memory and storage hierarchy. These levels are differentiated from each other by access time, with both levels located within the more than two orders of magnitude between the latencies of off-chip DRAM (~80ns) and NAND Flash (20µs).

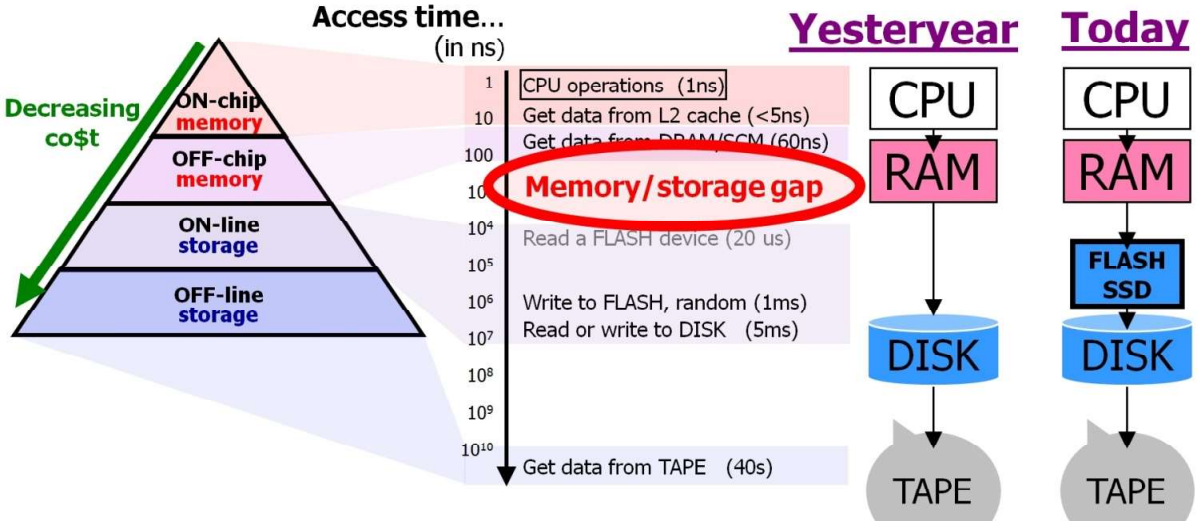

Figure 1 – Storage Class Memory [4-5] can be thought of as the realization that many emerging alternative nonvolatile memory technologies – such as Phase Change Memory (PCM) [1-3], Resistance RAM (RRAM), and Spin-Torque-Transfer Magnetic RAM (STT-MRAM) – can potentially offer significantly more than Flash, in terms of higher endurance, significantly faster performance, and direct-byte access capabilities.

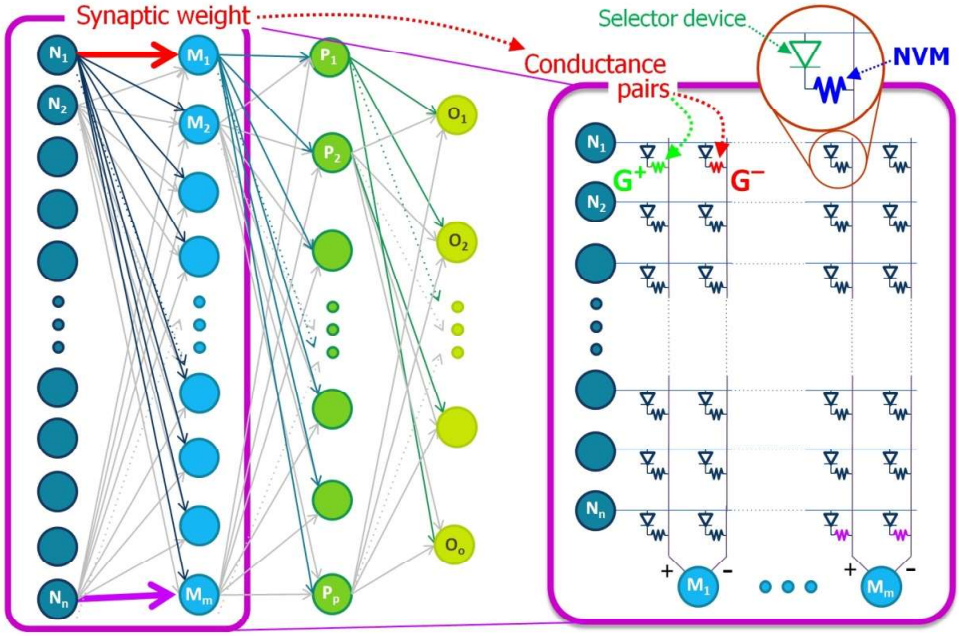

Figure 2 – Neuro-inspired non-Von Neumann computing [9-11], in which neurons activate each other through dense networks of programmable synaptic weights, can be implemented using dense crossbar arrays of nonvolatile memory (NVM)[1-4] and selector [6-8] device-pairs.

3. Neuromorphic Computing

Such large arrays of NVM can also be used in non-Von Neumann neuromorphic computational schemes, with device conductance serving as the plastic (modifiable) "weight" of each "native" synaptic device (Figure 2). This is an attractive application for these devices, because while many synaptic weights are required, requirements on yield and variability can be more relaxed. However, work in this field has remained highly qualitative in nature, and slow to scale in size.

I will discuss our recent work towards large crossbar arrays of NVM for both of these applications. After briefly reviewing earlier work on PCM [1-3], SCM [4-5], and access devices [6] based on copper-containing Mixed-Ionic-Electronic-Conduction (MIEC) [7-8], I will discuss our recent work on quantitatively assessing the engineering tradeoffs inherent in NVM-based neuromorphic systems [9-11].

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