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Structural and Electrical Characterization of Epitaxial Ge Thin Film on Si (001) Formed by Sputtering

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Abstract

We have characterized sub-10 nm heteroepitaxial Ge film on Si (001) heated sputtering crystallographically and electrically. Smooth surface was preserved with roughness root mean square (RMS) of 0.54 nm, while X-ray diffraction (XRD) and transmission electron microscopy (TEM) indicated epitaxial growth of the Ge on Si. *C-V* measurements of the TaN/Ge/n-Si diode indicate that built-in potential is 0.32 V, which is consistent with the model assuming band alignment of Ge/Si heterostructure.

1. Introduction

Tunnel field effect transistors (TFETs) are a promising candidate for low power consumption transistors. Enhancement of tunnel probability to provide sufficient on-current is a key challenge for Si-based TFETs. We have previously reported a novel TFET that has an $Si_{0.7}Ge_{0.3}$/Si heterojunction multilayer with a sub-10 nm thickness [1]. Replacing $Si_{0.7}Ge_{0.3}$ with pure Ge having smaller band gap is effective to enhance the tunnel probability further [2]. Epitaxial Ge films are usually deposited by chemical vapor deposition (CVD). However, the CVD growth of Ge having a sub-10 nm thickness results in problematic island growth on Si surface with significant roughness [3,4]. We have focused on DC magnetron sputtering of thin Ge film [5,6], and succeeded in depositing sub-10nm thick epitaxial Ge on Si with significant surface smoothness [7].

In this study, the Ge thin film grown on Si by sputtering is characterized by structural and electrical analysis. In the first part of this study, we have investigated the surface morphology and crystallinity of the epitaxial Ge thin film deposited by sputtering. Then in order to confirm the integrity of the Ge/Si interface, *C-V* measurement was performed to characterize the epitaxial Ge thin film with regard to the Ge/Si band alignment.

2. Structural characterization of Ge/Si

B-doped Si (001) substrates with 1-100 Ωcm resistivity are used. First, the substrates are cleaned using diluted HF acid (1%). Then, we grow a 6 nm Ge layer on the substrates using DC magnetron sputtering. The growth temperature is 350 °C. After deposition, the rapid thermal annealing (RTA) is performed at 720 °C to improve crystallinity.

Fig. 1 shows the atomic force microscopy (AFM) image of the Ge surface. Island-like morphology is not observed in the Ge film and a smooth surface is preserved. Roughness root mean square (RMS) measured by AFM is 0.54 nm, which is much smaller than that of 10 nm Ge grown at 400 °C by low pressure CVD (LPCVD) (RMS is 4.46 nm)[3]. Fig. 2 shows the 2θ–ω XRD spectra for the Ge film. Peaks assigned as Ge (111), (220), (311), and (331) do not appear. Ge (004) peak is only observed in the 2θ range between 20 and 80 °, which suggests that the Ge film is single crystalline. Fig. 3 shows the cross section TEM image of the Ge/Si heterostructure. In the TEM image, lattice continuity is maintained, which indicates that the Ge films are grown epitaxially. These results suggest that the epitaxial Ge thin film with smooth surface on Si (001) is successfully obtained without island formation.

3. Electrical characterization of Ge/Si

In order to examine the integrity of the Ge/Si heterostructure with regard to the Ge/Si band alignment, built-in potential (V_{bi}) of Schottky diodes fabricated both on Si and Ge/Si is evaluated. We fabricate TaN/Ge/n-Si diodes for *C-V* characteristics measurement by the process shown in Fig.4. Phosphorus-doped Si (001) substrates with 1-5 Ωcm resistivity are used. After the isolation process by the local oxidation of silicon (LOCOS) method, Ge/n-Si heterojunction is fabricated by epitaxial growth utilizing the Ge sputtering method as mentioned above. The Ge film thickness is 6 nm. TaN is deposited subsequently to form Schottky diode. The junction area of the diode is 100 μm × 100 μm. To extract the contribution of the Ge/Si heterostructure, TaN/n-Si Schottky diodes are also prepared for comparison.

Fig. 5 shows plots of $1/C^2$ - V. Both the TaN/Ge/n-Si and TaN/n-Si diodes show linear relationship. The built-in potential (V_{bi}) is obtained by extrapolating the linear fit to the voltage axis. Slopes of the linear fit also provide dopant concentration (N_D) in the n-Si substrates, which are used to calculate Fermi level (E_f) in Si for the discussion later. The V_{bi} values obtained for 10 samples for each case of the TaN/Ge/n-Si and TaN/n-Si diodes are summarized in Fig. 6. Averages are 0.49 and 0.32 V for TaN/n-Si and TaN/Ge/n-Si, respectively. Fig. 7 shows models of band profiles for the TaN/Ge/n-Si and TaN/n-Si diodes assuming flat band condition, in which V_{bi} is given by the difference between E_f in n-Si and that in TaN. Note that the Schottky barrier height (SBH) values at the TaN/Ge [8] and TaN/Si [9] interfaces are taken from the measured values reported previously. The V_{bi} values obtained from the *C-V* measurement and the model in Fig.7 are summarized in Table 1. Clearly seen, the measured V_{bi} for the TaN/Ge/n-Si and TaN/n-Si diodes are consistent with those from the model. Namely, the heterostructure of the thin Ge on Si exhibits significant consistency with the Si/Ge band alignment.

4. Conclusions

The sub-10 nm heteroepitaxial Ge film on Si (001) grown by the heated sputtering method was characterized crystallographically and electrically. It is confirmed that the Ge film is grown epitaxially with significantly smooth surface. The V_{bi} obtained from $1/C^2 - V$ plot for the TaN/Ge/n-Si diode agrees well with the model assuming the Ge/Si band alignment. These results support the effective-

ness of the heated sputtering method for introducing the Ge/Si heterostructure into TFETs.

Acknowledgements

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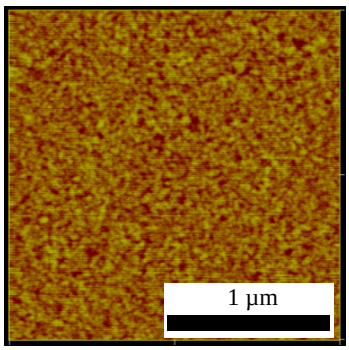

Fig. 1. The AFM image of Ge surface after RTA at 720 °C for grown at 350 °C . Roughness RMS is 0.54 nm.

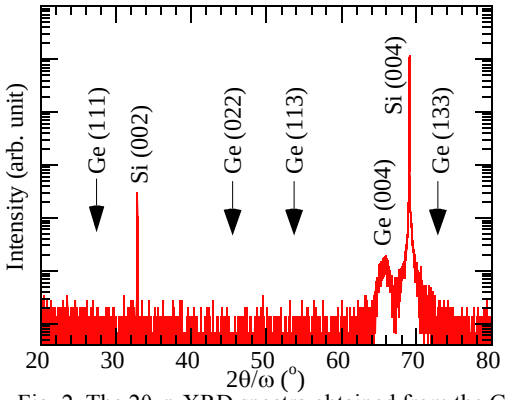

Fig. 2. The 2θ-ω XRD spectra obtained from the Ge film grown at 350 °C with 720 °C RTA.

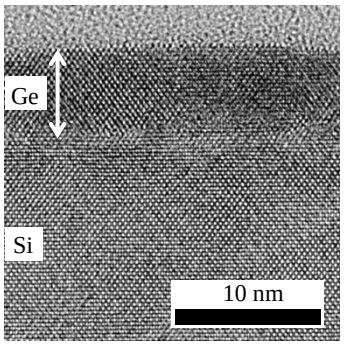

Fig. 3. Cross section TEM image of the Ge film grown at 350 °C with 720 °C RTA.

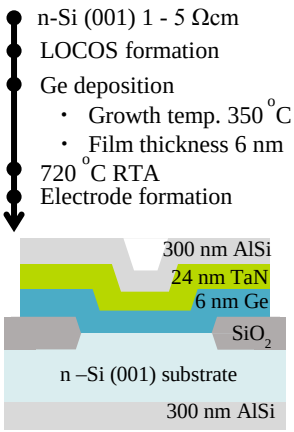

Fig. 4. Process flow and schematic of cross section of TaN/Ge/n-Si diode.

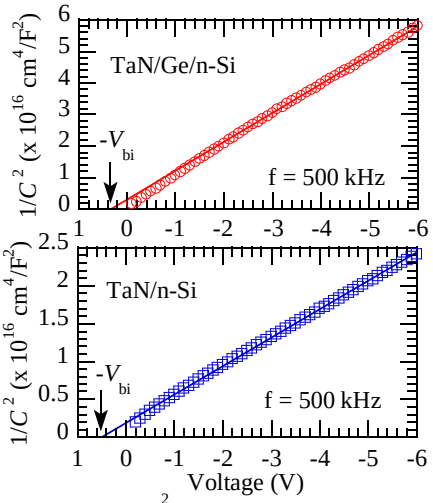

Fig. 5. $1/C^2$ vs V plot of TaN/Ge/n-Si and TaN/n-Si diodes.

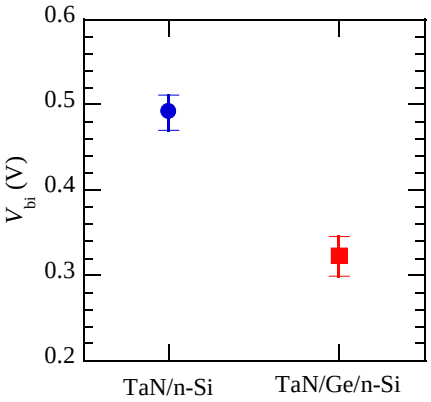

Fig. 6. Summary of V_{bi} of diodes with and without Ge layer. Error bars indicate the minimum and maximum values in 10 samples.

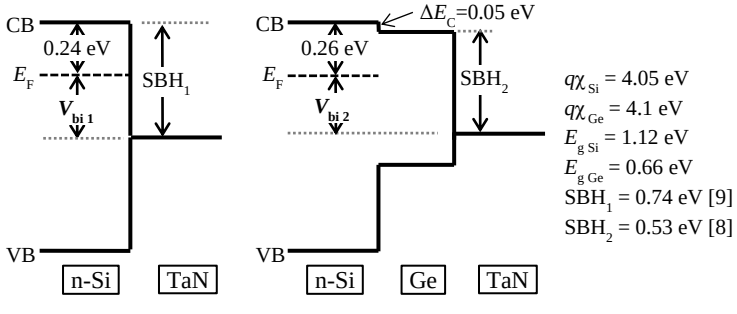

Fig. 7. Band alignment of TaN/n-Si and TaN/Ge/n-Si junction for flat band condition. SBHs are taken from reported value [8,9].

Table 1. Comparison of V_{bi} between measurement and model.

	$V_{bi\,1}$: TaN/n-Si	$V_{bi\,2}$: TaN/Ge/n-Si
Model (Fig.7)	0.50 V	0.32 V
Measured (Fig.6)	0.49 V	0.32 V