Extended Abstracts of the 2016 International Conference on Solid State Devices and Materials, Tsukuba, 2016, pp649-650

PS-1-03

Formation Technology of Flat Surface after Selective-Epitaxial-Growth on Ion-implanted (100) Oriented Thin SOI Wafers

K. Furukawa[1], A. Teramoto[2], R. Kuroda[1], T. Suwa[2], K. Hashimoto[2], S. Sugawa[1,2],
D. Suzuki[3], Y. Chiba[3], K. Ishii[3], A. Shimizu[3], and K. Hasebe[3]
[1] Graduate School of Engineering, Tohoku Univ., [2] New Industry Creation Hatchery Center, Tohoku Univ.,
6-6-11-811, Aza-Aoba, Aramaki Aobaku, Sendai, Miyagi 980-8579, Japan
Phone: +81-22-795-4833 E-mail: kiichi.furukawa.p7@dc.tohoku.ac.jp
[3] Tokyo Electron Tohoku Limited Yamanashi Regional Office,
650 Mitsuzawa, Hosakacho, Nirasaki, Yamanashi 407-0192, Japan

Abstract

This paper gives some experimental analyses of the surface roughness after silicon selective-epitaxial-growth on ion-implanted (100) oriented thin silicon on insulator (SOI) wafers. Both n- and p-type dopants with several impurity concentrations are examined. The combination of solid-phase epitaxy and the plasma flattening treatment is highly effective to obtain a flat surface.

1. Introduction

Selective-epitaxial-growth (SEG) [1] is a key component in semiconductor manufacturing process. Extension of source and drain for the contact formation of fin-type MOSFETs [2] is a well-known example of SEG. Low temperature SEG on ion-implanted silicon is an attractive process in order to form an ultra-shallow or steep p-n junction for fin-type MOSFET as well as tunnel MOSFET [3, 4] (see Fig. 1). For these applications, the surface roughness of SEG films and the diffusion of impurities from the substrate into the films become major concerns as well as the quality of the films because they directly affect the electric characteristics of devices. In this paper, we examined the impact of process conditions of vapor-phase epitaxy (VPE) and solid-phase epitaxy (SPE) to the surface roughness of SEG films formed on thin SOI wafers doped with high concentration impurities. Through the experiments, a process technology to obtain a flat surface after SEG is proposed.

2. Vaper Phase Epitaxy

Fig. 2 shows the sequence of VPE. SiH_4/Cl_2 gases were used for deposition/etching to obtain high selectivity. Low temperature of 550°C was used to suppress the diffusion of impurities from SOI layer. Fig.3 shows the fabrication flow of sample wafers. In this paper, (100) oriented SOI p-type (Boron $2.0\times10^{15}cm^{-3}$) thin wafers (from 30 nm to 60nm of SOI and 145nm of bottom oxide (BOX) layers) were used and all samples were fabricated with this flow. In the ion-implanted process, As^+ and BF_2^+ ions were implanted with 10keV, and activation annealing was carried out.

Table I shows the variation of the film thickness of SOI layer with several impurity concentrations. In the case of p-types, there was no deviation of the film thickness and no impurity concentration dependency. In contrast, in the n-types, the original SOI layer was etched with high impurity concentration. Also, there was impurity concentration dependency.

To clarify the mechanism that n-types were etched or little deposited, we performed the pretreatment, deposition, and etching phase separately with n-type of As^+ $2.0\times10^{14}cm^{-2}$ and p-type no ion-implanted one. Figs. 4 show the deposition/etching rate of each phase. In the pretreatment phase, the etching speed of n-type was larger than that of p-type by 3 times. In the deposition phase, the deposition rate was almost the same, but the incubation time of n-type was much longer than that of p-type. The estimated incubation time was longer than 10 minutes which is the deposition time in this VPE. Therefore, Si film was not formed on the n-types.

Fig. 5 shows the Secondary-Ion-Mass-Spectroscopy (SIMS) depth profile of ^{11}B of the p-type of BF_2^+ $2.0\times10^{14}cm^{-2}$. The peek concentration was higher than $10^{19}cm^{-3}$ and the slope of the diffusion was approximately 2.5nm/decade. It is close to the value of 1nm/decade which was reported as an example of the epitaxial-channel [4] for device applications.

Figs. 6 show the AFM images of p-types. The roughness increased as the concentration of BF_2^+ ions. Figs. 7 show the AFM images (top views) of n-types after 50 minutes of deposition with several impurity conditions. The black/white point indicates lower/higher level in each image. Many black squares were observed and the number of squares increases as the concentration of As^+ ions. Also, every square aligns along with the same direction. This implies that (111) facet appeared during VPE.

3. Solid Phase Epitaxy

Fig. 8 shows the sequence of SPE. The deposition temperature was changed from 550°C to 400°C and annealing process was carried out for SPE. Figs. 9 show the AFM images of n- and p-types after SPE. Very flat surface was observed with no ion-implanted one. However, the surface becomes so rough with ion-implanted ones that the film thickness could not be measured correctly with spectroscopic-ellipsometry. Figs. 10 show the AFM images just after the amorphous-Si deposition. At this time, the surface was not roughened. Therefore the rough surface was thought to be formed by the migration of deposited a-Si during the following annealing.

In Fig. 11, an oxidation process to form a native SiO_2 capping layer on the surface was added. Fig. 12 (a) show the AFM images with the modified SPE. The roughness was drastically reduced with SiO_2 cap .The 1nm of SiO_2 cap prevents Si atoms from migrating during the annealing.

4. Low Temperature Plasma Flattening Treatment

Also, we performed the H_2-Xe low temperature plasma flattening treatment [5]. 10/90% of H_2/Xe plasma was used. Fig. 12 (b) shows the AFM image after 400°C and 1minute of plasma treatment. The roughness was reduced a little more. Fig. 13 shows the variation of Ra values at each process point. Ra values of both n- and p-type reduced with plasma treatment. Fig. 14 shows SIMS depth profile of ^{11}B and ^{16}O of the p-type flattened one (the sample shown in Fig. 12 (b)). The slope of diffusion was 1.5nm/decade and there were little O atoms detected, which means there were little defects in the SPE film.

5. Conclusion

We investigated the surface roughness after VPE and SPE on both n- and p-types. From our results, SPE should be used to obtain a flat surface and the H_2-Xe plasma treatment is effective to reduce the roughness. For device applications, we consider the value of Ra less than 0.2nm is applicable for S/D extension of fin-type MOSFET and the channel-gate insulator interface for tunnel-MOSFET.

References

[1] J. L. Regorini, et al., Journal of Crystal Growth, 99, 505-512, 1989
[2] J. Kedzierski, et al., IEEE Trans. Electron Devices, 50, 4, 952-158, 2003
[3] K. Furukawa, et al., Jpn. J. Appl. Phys., 4S, 55, 04ED12-1-7, 2016
[4] Y. Morita, et al., IEDM Tech Dig., 243, 2014
[5] T. Suwa, et al., ECS Trans., 66, 5, 277-283, 2015

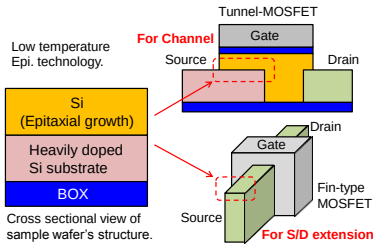


Fig.1 Examples of SEG applications.

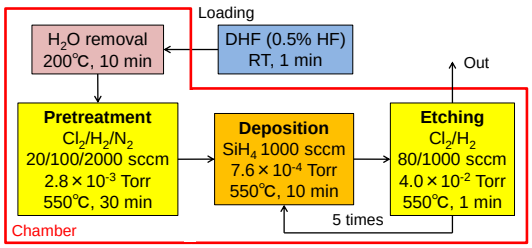


Fig.2 Sequence of selective epitaxial growth (vapor-phase).

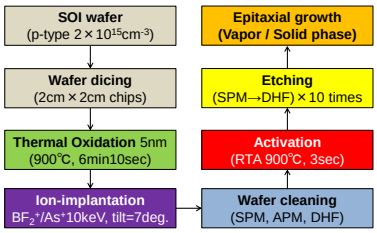
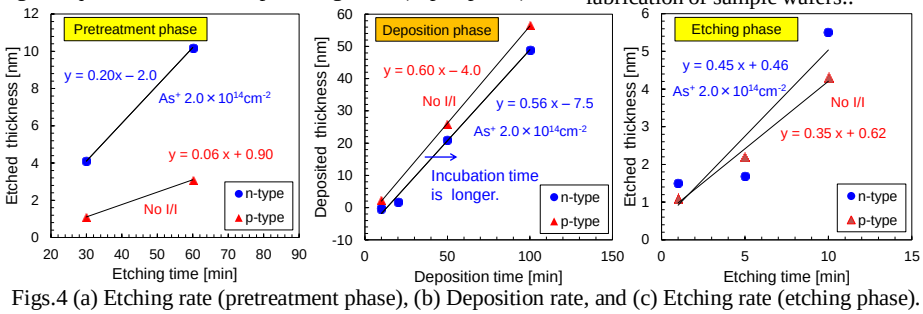


Fig.3 Process flow diagram of the fabrication of sample wafers..

Table I Thickness before and after Epi.

Wafer ID	Ion-Implantation dose concentration	Before Epi. SOI [nm]	Before Epi. X^2	After Epi. SOI [nm]	After Epi. X^2	Delta [nm]
A-1	BF_2^+ 2.0×10^14 cm^-2	31.7	0.46	44.7	0.71	+ 13.0
A-2		31.7	0.55	45.1	0.74	+ 13.4
B-1	BF_2^+ 5.0×10^13 cm^-2	31.6	0.50	46.8	0.77	+ 15.1
B-2		30.1	0.53	42.9	0.77	+ 12.7
C-1	As^+ 2.0×10^14 cm^-2	26.8	1.54	19.0	0.38	- 7.7
C-2		30.8	1.16	21.1	0.37	- 7.4
D-1	As^+ 5.0×10^13 cm^-2	30.3	0.42	32.5	0.32	+ 2.2
D-2		29.4	0.46	30.9	0.31	+ 1.4
E-1	No Ion-implantation (p-type)	30.5	0.58	44.6	0.82	+ 14.0
E-2		30.0	0.55	44.2	0.78	+ 14.2



Figs.4 (a) Etching rate (pretreatment phase), (b) Deposition rate, and (c) Etching rate (etching phase).

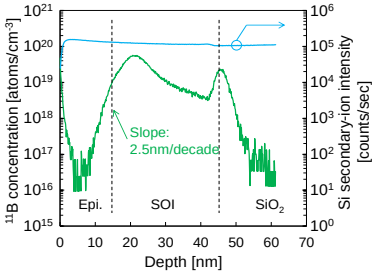
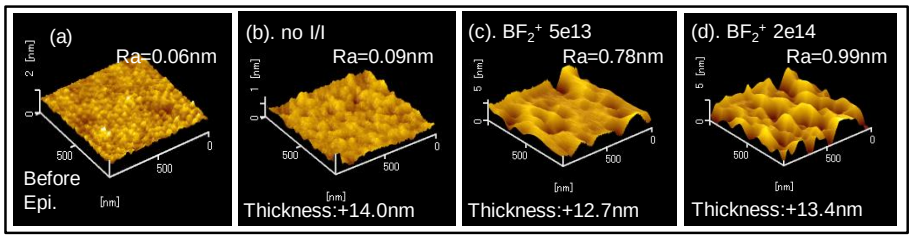
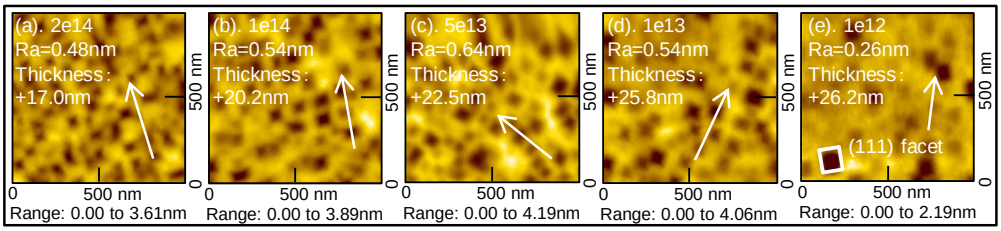


Fig.5 SIMS depth profile of ^{11}B (p-type BF_2^+ 2×10^14cm^-2).



Figs.6 AFM images of (a) before Epi., (b) no I/I, (c) BF_2^+ 5×10^13cm^-2, and (d) BF_2^+ 2×10^14cm^-2.

→Figs.7 AFM images of top-view with As^+ of (a) 2×10^14, (b) 1×10^14, (c) 5×10^13, (d) 1×10^13, and (e) 1×10^12 cm^-2.
View area: 1um×1um,
Black spot: Lower, White spot: Higher



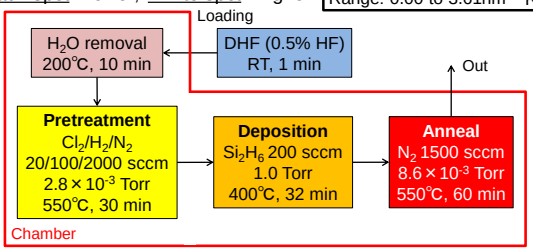
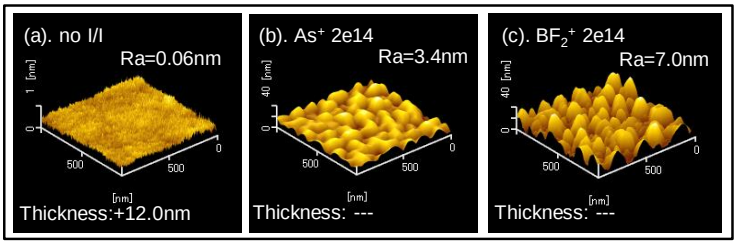


Fig.8 Sequence of low temperature solid phase epitaxy.



Figs.9 AFM images of (a) no I/I, (b) As^+ 2×10^14cm^-2, and (c) BF_2^+ 2×10^14cm^-2.

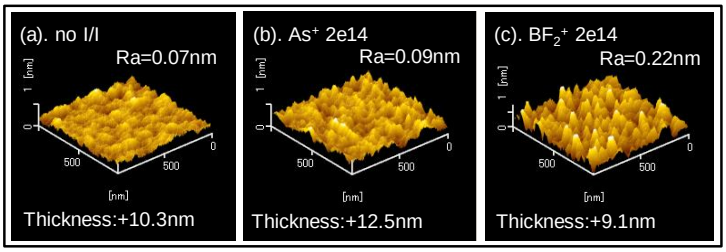


Fig.10 AFM images of as-deposition surface of amorphous silicon.

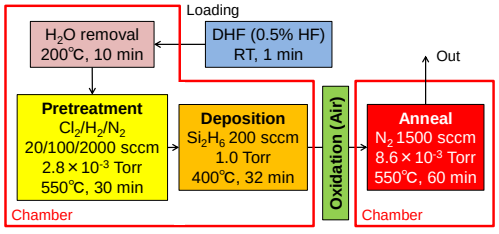
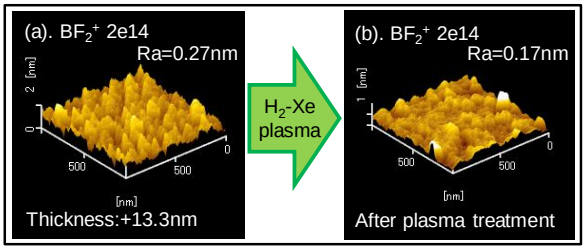


Fig.11 Sequence of LT-SPE with a SiO_2 cap formation.



Figs.12 AFM images of modified SPE with SiO_2 cap.
(a) after SiO_2 removal and (b) after plasma flattening treatment.

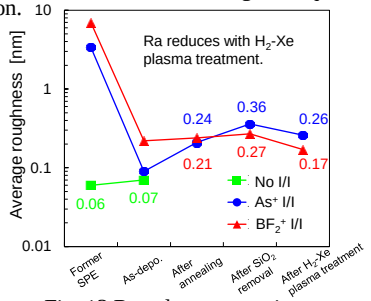


Fig. 13 Ra values comparison.

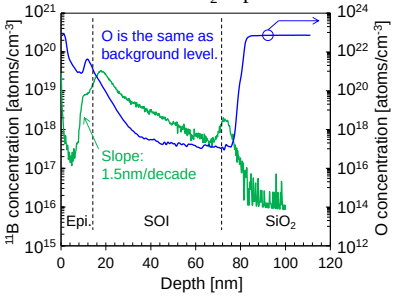


Fig.14 SIMS depth profile of ^{11}B and ^{16}O (p-type BF_2^+ 2×10^14cm^-2 after flattened).