Extended Abstracts of the 2016 International Conference on Solid State Devices and Materials, Tsukuba, 2016, pp651-652

PS-1-04

Impact of $Si_xGe_{1-x-y}Sn_y$ interlayer on reduction in Schottky barrier height of metal/*n*-Ge contact

Akihiro Suzuki[1, 2], Shota Toda[1], Osamu Nakatsuka[1], Mitsuo Sakashita[1], and Shigeaki Zaima[1, 3]

[1]Graduate School of Engineering, Nagoya University, Furo-cho, Chikusa-ku, Nagoya 464-8603, Japan
[2]Research Fellow of Japan Society for the Promotion of Science, Tokyo 102-8803, Japan
[3]Institute of Materials and Systems for Sustainability, Nagoya University, Furo-cho, Chikusa-ku, Nagoya 464-8603, Japan
Phone: +81-52-789-3819, E-mail: asuzuki@alice.xtal.nagoya-u.ac.jp

Abstract

A Schottky barrier height (SBH) as low as 0.18 eV has been achieved by inserting a lattice-matched $Si_{0.04}Ge_{0.95}Sn_{0.01}$ ternary alloy interlayer at Al/*n*-Ge interface. A smaller strain with lattice matching of a $Si_xGe_{1-x-y}Sn_y$ interlayer to Ge leads to a lower SBH of metal/*n*-Ge contact.

1. Introduction

One of the serious issues for the practical realization of high performance Ge-channel metal-oxide-semiconductor field effect transistor (MOSFET) is reduction of parasitic resistance. Especially, the reduction of the contact resistivity for metal/*n*-Ge interface is generally difficult because of a high Schottky barrier height (SBH) for *n*-Ge regardless of the metal work function due to a well-known Fermi level pinning (FLP) phenomenon. Origins of FLP at metal/Ge interface are discussed with metal-induced-gap-states (MIGS) and disorder-induced-gap-states (DIGS) models. MIGS is attributed to the penetration of electron wave function in a metal into semiconductor. On the other hand, DIGS is attributed to the disorder of atomic arrangement such as dangling bonds at the interface. Some technologies for reducing SBH of metal/*n*-Ge contact were previously reported, using wide bandgap dielectric interlayer [1–3], epitaxial metal [4, 5], amorphous metal nitride interlayer [6], and $Ge_{1-x}Sn_x$ interlayer [7]. However, the technique of controlling FLP and SBH still has to be developed to reduce the contact resistivity for practical applications.

Here, we are focusing on the insertion of an epitaxial $Si_xGe_{1-x-y}Sn_y$ ternary alloy layer at metal/Ge interface. The energy band structure and lattice constant of $Si_xGe_{1-x-y}Sn_y$ can be independently controlled by contents of each element. Recently, our group has previously reported the high thermal robustness and the energy band structure of lattice-matched $Si_xGe_{1-x-y}Sn_y$/Ge heterostructure [8, 9]. $Si_xGe_{1-x-y}Sn_y$ lattice-matched to Ge with a content ratio x/y of 3.7 realizes no-misfit epitaxial layer on Ge. That promises the high crystallinity and minimizing the dangling bond density at the $Si_xGe_{1-x-y}Sn_y$/Ge interface compared to a lattice-mismatched $Ge_{1-x}Sn_x$/Ge one [7]. Additionally, we expect that a $Si_xGe_{1-x-y}Sn_y$ interlayer would suppress MIGS because its energy bandgap (E_g) is larger than that of Ge when the Si content increases. However, there is no report about the effect of $Si_xGe_{1-x-y}Sn_y$ interlayer on SBH of metal/Ge contact. In this report, we investigated the impact of epitaxial $Si_xGe_{1-x-y}Sn_y$ interlayer on the SBH reduction of metal/*n*-Ge contact.

2. Sample preparation

After chemical and thermal cleaning *n*-Ge(001), a 6–8 nm-thick $Si_xGe_{1-x-y}Sn_y$ epitaxial layer was grown on the Ge substrate with molecular beam epitaxy system. The deposition temperature was 200 °C. Contents of each element in $Si_xGe_{1-x-y}Sn_y$ layers were estimated using X-ray photoelectron spectroscopy. Two kinds of $Si_xGe_{1-x-y}Sn_y$ layers with Si and Sn contents (x, y) of (4%, 1%) and (15%, 6%) were prepared. The expected lattice constant of $Si_{0.04}Ge_{0.95}Sn_{0.01}$ is almost completely matched to Ge, while that of Sn-rich $Si_{0.15}Ge_{0.79}Sn_{0.06}$ is 0.28% larger than Ge. After taking out the samples to atmosphere, native oxide on the $Si_xGe_{1-x-y}Sn_y$ surface was chemically removed. Then, Al electrodes were immediately deposited on the $Si_xGe_{1-x-y}Sn_y$ surface and backside with vacuum evaporation method to prepare Al/$Si_xGe_{1-x-y}Sn_y$/*n*-Ge Schottky diodes. An Al/*n*-Ge diode without $Si_xGe_{1-x-y}Sn_y$ was also prepared for comparison.

3. Results and discussion

The *in-situ* reflection high energy electron diffraction (RHEED) observation revealed the epitaxial growth of $Si_xGe_{1-x-y}Sn_y$ layers on Ge as shown in **Fig. 1**. For the $Si_{0.04}Ge_{0.95}Sn_{0.01}$ layer, a sharp pattern with the 1/2 order streak related to the surface reconstruction is clearly observed (**Fig. 1(a)**). On the other hand, for the $Si_{0.15}Ge_{0.79}Sn_{0.06}$ layer, spotty pattern related to the three dimensional growth is observed (**Fig. 1(b)**). These results indicate a superior surface flatness of the lattice-matched $Si_{0.04}Ge_{0.95}Sn_{0.01}$ layer to that of Sn-rich $Si_{0.15}Ge_{0.79}Sn_{0.06}$ compressively strained on Ge.

Figure 2 shows the in-plane X-ray diffraction (XRD) profiles of $Si_xGe_{1-x-y}Sn_y$/Ge samples and a Ge substrate. Broadening of the tail profile of the Ge220 Bragg reflection is significantly observed just for the $Si_{0.15}Ge_{0.79}Sn_{0.06}$/Ge sample. This result indicates that the crystallinity of the Sn-rich $Si_{0.15}Ge_{0.79}Sn_{0.06}$ layer is inferior to the lattice-matched $Si_{0.04}Ge_{0.95}Sn_{0.01}$ due to any lattice distortion and/or dislocation, which is consistent with the RHEED result.

Current density-voltage (*J-V*) measurement was performed for Al/$Si_xGe_{1-x-y}Sn_y$/*n*-Ge and Al/*n*-Ge Schottky diodes at various temperatures. **Figure 3** shows the *J-V* characteristics of all diodes measured at 300 K. While a rectifying behavior is clearly observed in the Al/*n*-Ge diode, the rectifying behavior is significantly weak in the Al/$Si_{0.15}Ge_{0.79}Sn_{0.06}$/*n*-Ge diode. Interestingly, a complete ohmic behavior is observed in the diode with the $Si_{0.04}Ge_{0.95}Sn_{0.01}$ interlayer. For this diode, a rectifying behavior appeared just at a low temperature region below 150 K. (*not shown*). These *J-V* characteristics of Al/$Si_xGe_{1-x-y}Sn_y$/*n*-

Ge diodes indicate a practical reduction in SBH compared to Al/n-Ge contact.

The Arrhenius plots of the saturation current density (J_S) for the SBH estimation are shown in **Fig. 4**. We confirmed that the thermionic emission current conduction is dominant from the ideality factor in forward J-V characteristics used for the estimation of J_S at each temperature. **Figure 5** shows SBHs estimated from slopes of the Arrhenius plots for Al/$Si_xGe_{1-x-y}Sn_y$/n-Ge and Al/n-Ge diodes. SBHs of various metal/n-Ge contact are also summarized as a function of the metal work function for comparison [10]. The SBHs of Al/$Si_xGe_{1-x-y}Sn_y$/n-Ge diodes are lower than that of the Al/n-Ge contact (0.69 eV), and the lowest SBH of 0.18 eV was achieved in the Al/$Si_{0.04}Ge_{0.79}Sn_{0.01}$/$n$-Ge diode.

According to previous theoretical calculation, E_g of $Si_{0.04}Ge_{0.79}Sn_{0.01}$ and $Si_{0.15}Ge_{0.79}Sn_{0.06}$ at 0 K are estimated to be 0.72 and 0.73 eV, which are close to that of Ge (0.70 eV) [11]. Hence, $Si_{0.04}Ge_{0.79}Sn_{0.01}$ and $Si_{0.15}Ge_{0.79}Sn_{0.06}$ interlayers with such a small E_g in this study would hardly alleviate FLP as a wide-bandgap dielectric layer like Al_2O_3 and TiO_2 [2]. Considering this fact, we suggest that a $Si_xGe_{1-x-y}Sn_y$ interlayer plays a role which shifts the pinning position at Al/n-Ge interface towards the conduction band edge of Ge, leading to the reduction in SBH of metal/n-Ge contact.

4. Conclusions

We investigated the impact of a $Si_xGe_{1-x-y}Sn_y$ ternary alloy interlayer on the SBH of metal/n-Ge contact. By inserting $Si_{0.04}Ge_{0.79}Sn_{0.01}$ and $Si_{0.15}Ge_{0.79}Sn_{0.06}$ layers at Al/n-Ge interface, SBHs can be reduced to 0.18 and 0.23 eV respectively. We successfully demonstrated that a lattice-matched $Si_xGe_{1-x-y}Sn_y$ interlayer effectively reduces the SBH, which promises reducing the contact resistivity of metal/n-Ge contact with providing appropriate energy band structure, controllable Fermi level, and high thermal robustness for Ge-channel n-MOSFET applications.

Acknowledgements

Authors acknowledge Prof. K. Saraswat and Prof. Y. Nishi at Stanford University for our private communication. This work was partly supported by the Grant-in-Aid for Scientific Research (B) (No. 15H03565) of JSPS in Japan.

References

[1] T. Nishimura *et al.*, Appl. Phys. Exp. **1**, 051406 (2008).
[2] J. Lin *et al.*, Appl. Phys. Lett. **98**, 092113 (2011).
[3] G. Shine *et al*, in *Proc. SISPAD*, p. 69, Glasgow, Scotland, Sept. (2013).
[4] K. Yamane *et al.*, Appl. Phys. Lett. **96**, 162104 (2010).
[5] T. Nishimura *et al.*, Microelectron. Eng. **88**, 605 (2011).
[6] K. Yamamoto *et al.*, J. Appl. Phys. **118**, 115701 (2015).
[7] A. Suzuki *et al.*, Appl. Phys. Lett. **107**, 212103 (2015).
[8] T. Asano *et al.*, Solid-State Electron. **110**, 49 (2015).
[9] T. Yamaha *et al.*, Appl. Phys. Lett. **108**, 061909 (2016).
[10] T. Nishimura *et al.*, Appl. Phys. Lett. **91**, 123123 (2007) etc.
[11] P. Moontragoon *et al.*, J. Appl. Phys. **112**, 073106 (2012).

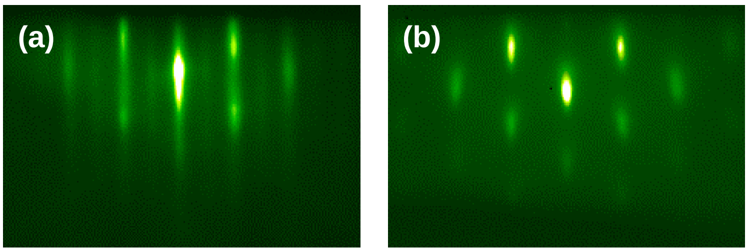

Fig. 1 *In-situ* RHEED patterns of (a) $Si_{0.04}Ge_{0.79}Sn_{0.01}$ and (b) $Si_{0.15}Ge_{0.79}Sn_{0.06}$ layers grown on Ge substrate.

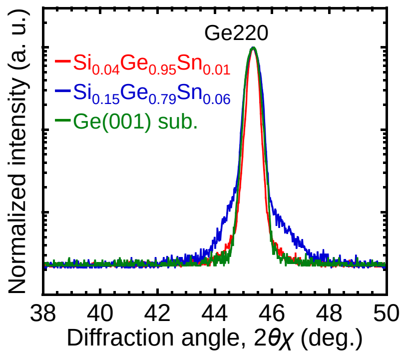

Fig. 2 In-plane XRD profiles of $Si_xGe_{1-x-y}Sn_y$/Ge samples and Ge substrate around the Ge220 Bragg reflection.

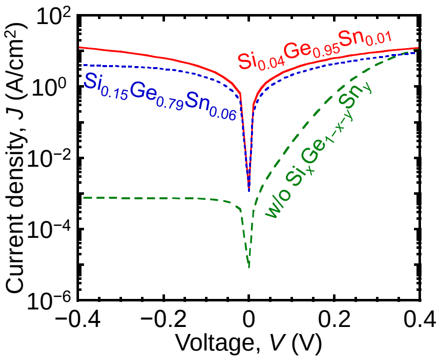

Fig. 3 J-V characteristics of Al/$Si_xGe_{1-x-y}Sn_y$/n-Ge and Al/n-Ge Schottky diodes at 300 K.

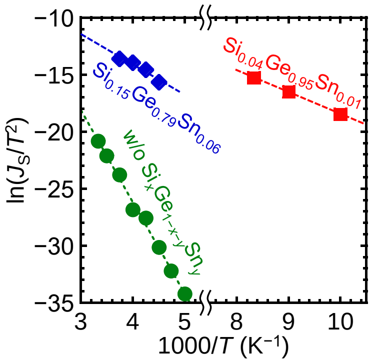

Fig. 4 Arrhenius plots of J_S/T^2 estimated from forward J-V characteristics of Al/$Si_xGe_{1-x-y}Sn_y$/n-Ge and Al/n-Ge Schottky diodes. T is the measurement temperature.

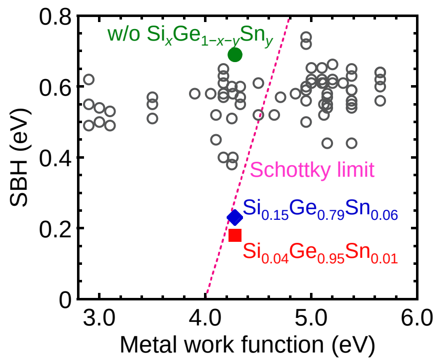

Fig. 5 The SBHs of Al/$Si_xGe_{1-x-y}Sn_y$/n-Ge and Al/n-Ge samples. SBHs of various metal/n-Ge contacts are also summarized as a function of the metal work function [10].