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Self-Aligned Deposition of Source/Drain Contact Metal with Electrodeposition Technique for High Performance Schottky Barrier Ge MOSFETs Fabrication

Dongyuan Zhai[1], Jinhong Jiang[1, 2], Junkang Li[1], Xiao Yu[1], Rui Zhang[1] and Yi Zhao[1, 3*]
[1]College of Information Science & Electronic Engineering, Zhejiang University, Hangzhou 310027, China
[2]The 51 th Research Institute of China Electronics Technology Group Corporation, Shanghai 201802, China
[3]State Key Laboratory of Silicon Materials, Zhejiang University, Hangzhou 310027, China
[*]E-mail: yizhao@zju.edu.cn

1. Introduction

With the continuous scaling of CMOS devices, Ge-based MOSFET has got extensive attentions for the high hole and electron mobility [1-4]. Unfortunately, the parasitic resistance, especially the source/drain (S/D) contact resistance (R_{sd}), could not be neglected any more for the aggressively scaled devices, which degrades the effectiveness of high mobility Ge channel [5]. Schottky Barrier Si and Ge MOSFETs are attracting a lot of attentions because of the shallow junction and the lower resistivity of silicide and germanide than doped Si and Ge [6, 7]. Fig. 1 shows the traditional process for Schottky Barrier MOSFETs, with the key point of selective etching of metal to silicide or germanide. However, there are two drawbacks in this process. The first one is the process complexity and the waste of resources of high temperature annealing during S/D formation and selective etching of un-reacted metal after S/D formation. The other drawback is that the resistivity of silicide or germanide is still not sufficiently low, compared with pure metals. In this study, with electrodeposition, a simple method to deposit metal [8, 9], the self-aligned Ni S/D contact is achieved, for the first time, for the Schottky Barrier Ge pMOSFETs. The process is greatly simplified compared with the traditional one. Meanwhile, because the sheet resisitance (R_{sh}) of germanide is substituted by the parallel resistance of germanide and pure metal, the R_{SD} is obviously reduced in these Ge Schottky Barrier devices.

2. Experimental

The device fabrication process is shown in Fig. 2. N-type Ge wafers with (100) orientation and resistivity of 0.1~1 Ω·cm were used. After the SiO_2 field oxide formation and the active area definition, the 30s ozone oxidation was used to form the GeO_x interfacial layer. The 15-nm-thick ALD Al_2O_3 was deposited at 300 ^oC, and the PDA was carried out at 400 ^oC for 30 min in N_2. The gate electrodes were deposited and patterned, and the Ni metal was electrodeposited at S/D. Finally, the Ni contact pads were formed.

3. Results and Discussion

As illustrated in fig 3, Ni can be selectively deposited at S/D region. Fig 3(a) and (b) show the energy band diagram for the S/D region and the gate region in contact with a solution respectively. During the electrodeposition, electrons can be accumulated in the cathode, which makes a higher electrical potential for the substrate, connected with the cathode, facilitating the transport of electrons form S/D region to the redox couples in the solution, while the electrons in Ge under gate oxide can't be transferred because of the high energy barrier of the gate oxide as shown in fig 3(b). Fig. 4(a) shows the SEM image of Ni deposited on the S/D region of a Ge pMOSFET. According to the Energy Dispersive Spectrometer (EDS) analysis (Fig. 4(b)), it is confirmed that Ni is selectively deposited only in the S/D regions. The Ni thickness could be precisely controlled by deposition time (Fig 4(c)). Fig. 5 shows the AFM image of a Ge substrate with electrodeposited Ni. It is observed that electrodeposited Ni shows a relatively flat surface, with grain size small than 50 nm (Fig. 5 (a)). Moreover, a direct evidence of selective growth of Ni by electrodeposition is confirmed from the step between the SiO_2 and the Ni/Ge regions (Fig. 5 (b)).

The electrodeposited Ni shows a good schottky contact with n-Ge, comparable with the evaporated Ni (Fig. 6(a)). At the same time, the electrodeposited Ni after annealing has much lower sheet resistance than the NiGe alloy in this study (Fig. 6(b)), which is vital for decreasing the R_{sd} of MOSFETs. Fig. 7 shows the I_d-V_d characteristics of the Ge pMOSFETs with electrodeposited Ni as contact metal. The device characteristic is comparable with that of traditional evaporation Ni metal source/drain device. However, due to the much lower R_{sh} of the electrodeposited Ni device than that of the device fabricated with the traditional germanide process as shown in Fig. 1(Fig. 6(b)), in the short channel device, the electrodeposited Ni device should have obvious advantage for enhancing the on-state current. Furthermore, the effectiveness of the electrodeposition process for other semiconductors, especially Si and III-V is also confirmed (Fig. 8). As shown in Fig. 9, the Schottky Barrier Si MOSFET with electrodeposited Ni shows the normal device operation. The selective Ni growth rate on Si and InP substrates could be controlled by the current during the electroplating (Fig. 10). It could be expected that various other well used metals (Co, Pt et al.) are able to be selectively electrodeposited on Ge, Si and III-V substrates for advanced CMOS devices fabrication.

4. Conclusions

With electrodeposition, the high performance Ni S/D Ge pMOSFETs have been demonstrated for the much lower R_{sd}. Due to the simple process and the effective R_{sd} reduction, this technique could be promising for S/D process in advanced CMOS technology with various semiconductor substrates, such as Si, Ge and III-V materials.

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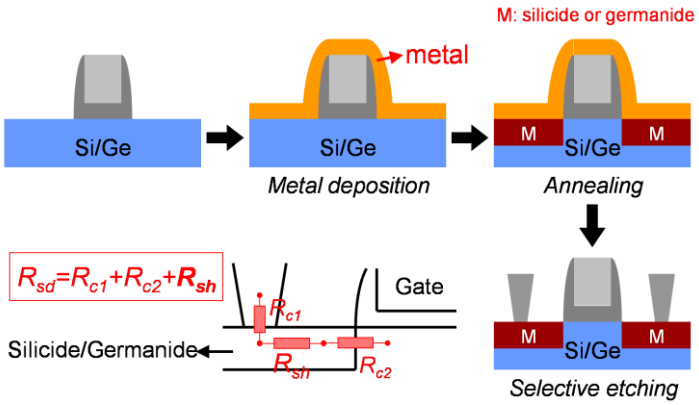

Fig. 1 Schematic diagram of silicide/germanide process.

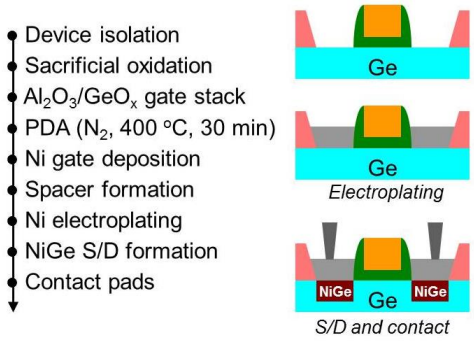

Fig.2 Process flow diagram of Ge pMOSFETs with electrodeposited Ni as contact metal in S/D region.

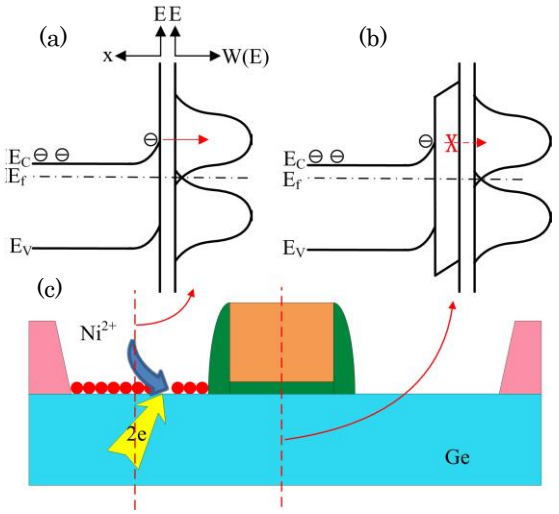

Fig. 3 The energy band diagram for the (a)S/D and (b)gate region in contact with a solution.(c)Schematic diagram of electrodeposition process for selective Ni deposition at S/D region of Ge MOSFET.

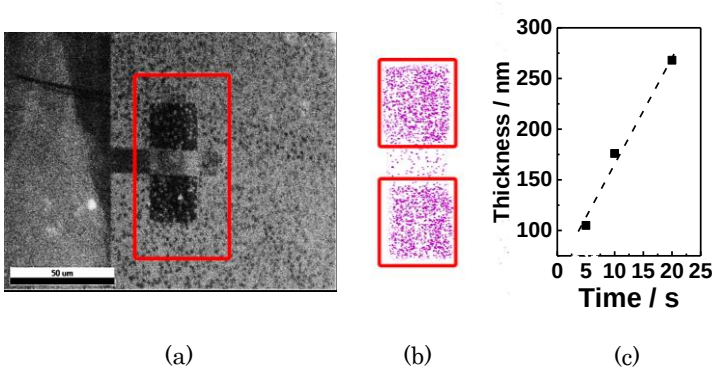

Fig. 4 (a) SEM image, (b) Mapping of Ni by EDS spectrum and (c) growth rate of selectively grown Ni at source/drain region of Ge pMOSFET.

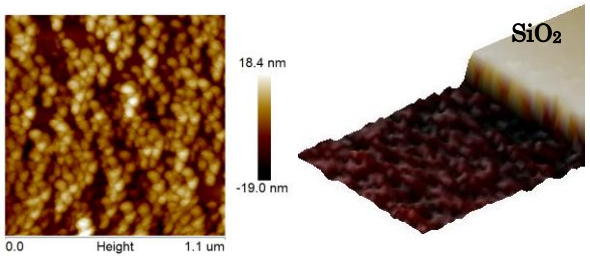

Fig. 5 AFM of (a) electroplated Ni film surface and (b) the step between Ni film and SiO_2 field oxide.

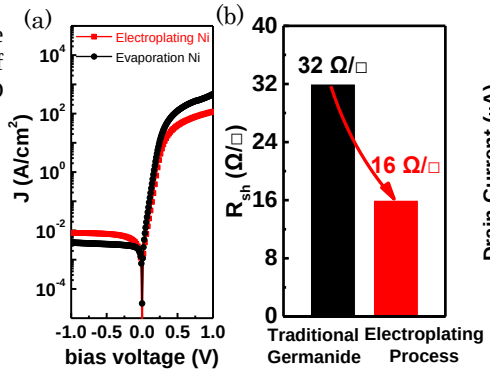

Fig.6 (a) I-V characteristics of electroplated Ni and thermally evaporated Ni with n- Ge and (b) sheet resistance(R_{sh}) comparison between electroplated Ni device and the traditional germanide device.

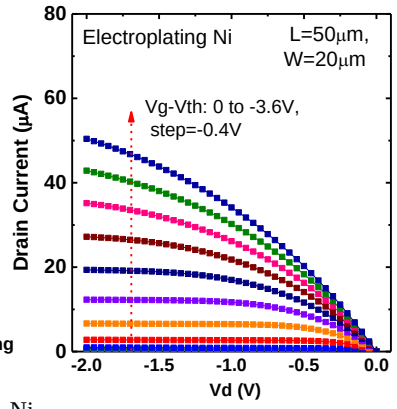

Fig.7 I-V characteristics of metal source/drain Ge pMOSFET with electrodeposited Ni.

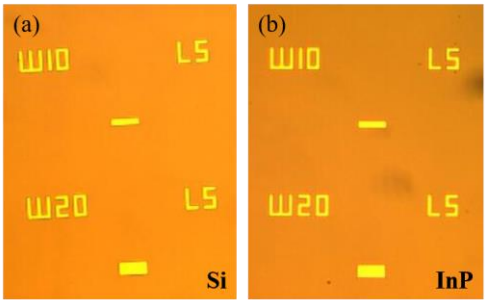

Fig.8 Microscope image of Ni selectively deposited on (a) Si and (b) InP substrates.

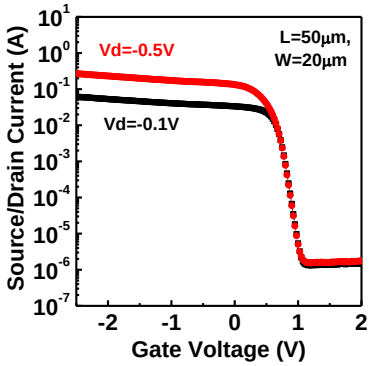

Fig.9 Device characteristics of metal source/drain Si pMOSFET with electrodeposited Ni.

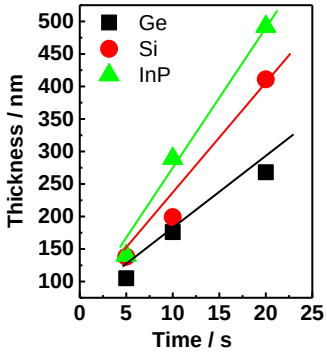

Fig. 10 Selective Ni growth on Si and InP substrates with electrodeposition.